JUNE 2008

CEDA Currents

IEEE Council on Electronic Design Automation

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The Council on Electronic Design Automation (CEDA) is an IEEE Council formed in 2005 by the IEEE Technical Activities Board. CEDA aims to bring together the EDA-related activities that run through many of the IEEE's societies, conferences and workshops. CEDA's responsibilities include sponsorship of several conferences and publications, such as ICCAD, DAC, and the Transactions on CAD and the sponsorship of a Distinguished Speaker Series. Members of CEDA include the IEEE Antennas and Propagation, Computer, Circuits and Systems, Electron Devices, Microwave Theory and Techniques, and Solid State Circuits Societies.

For more information on CEDA, go to www.ieee-ceda.org .

The 2008 MEMOCODE HW/SW Co-Design Contest

Contributed by Patrick Schaumont (Virginia Tech), Krste Asanovic (UC Berkeley) and James C. Hoe (Carnegie Mellon Univ.)

The second running of the MEMOCODE HW/SW Co-Design Contest concluded successfully on March 9, 2008. This annual contest was conceived for the MEMOCODE Conference (http://memocode-conference.com) to help highlight the issues distinct to HW/SW co-design and to expand the conference's emphasis on design and practice. On February 8, a "secret" design problem (involving AES and sorting) was revealed on the contest website, giving the contestants one month to produce working HW/SW co-designed solutions that compete in performance and in the elegance of design. By the conclusion of the contest, eleven entries from around the world (including US, Europe and Asia) were submitted out of the twenty-seven teams that started. This year's contest is organized by Patrick Schaumont (Virginia Tech), Krste Asanovic (UC Berkeley) and James C. Hoe (Carnegie Mellon University). The panel of judges comprises the three contest organizers, Kees Vissers (Xilinx) and Satrajit Chatterjee (Intel). This year's contest is sponsored by Nokia, Xilinx, Bluespec and IEEE CEDA. Please visit http://rijndael.ece.vt.edu/memocontest08 to see a description of the design problem and the contest rules.

The final design entries have been evaluated by the panel of judges, and the results of the contest are as follows. **Ranking**. Table 1 lists the affiliation and configuration of each finishing team. Table 2 lists, for each team, the overall speedup, the platform used, and the design languages used. The overall speedup is defined by the geometric mean of the set of testbench configurations, calibrated according to the platforms used. The table rows are sorted according to the overall speedup.

Table 1. Finishing Teams

Team ID	Affiliation	Size
sunita	Nanyang National University	8
uljana	Talinn University of Technology	4
brian	Brian Lindemann	1
vijay	AMD	1
marco	Politecnico Di Milano	13
rob	Old Dominion University	4
kermin	MIT	5
eric	Eric Simpson	1

Table 2. Performance Ranking

Team ID	Speedup	Platform	Language
kermin	1102.4	XUP	Bluespec
brian	100.2	XUP	C
marco	85.4	XUP	C + HDL
uljana	49.8	XUP	C + HDL
sunita (1)	41.1	XUP	C + HDL
vijay	33.0	XUP	C + HDL
rob	23.5	XUP	C + HDL
eric	12.8	XC2VP100	C + HDL
sunita (2)	11.0	XUP	C + Impulse C

All of the submissions were evaluated for correctness and performance by a panel of 5 judges. In addition, each judge evaluated the elegance of each design. Elegance is a subjective appreciation, and it considers factors such as cleverness of the algorithm, exploitation of parallelism, quality and clarity of the design documentation, and quality and clarity of the source code. The individual rankings were then combined, by majority voting, into a top-5 of elegant designs. The resulting elegance ranking is listed in table 3.

Table 3. Elegance Ranking

Rank	Team ID
1 (tie)	team kermin, team vijay
3	team brian
4	team marco
5	team sunita (2)

CEDA Currents is a publication of IEEE CEDA. Please send contributions to Jose L. Ayala, jayala@fdi.ucm.es or Rajesh Gupta.

Awards. Awards are defined in three categories: Higest Performance Design ($1000 prize), Most Efficient Design ($1000 prize), and a special Xilinx-sponsored prize for Best Figures of Merit Using a High Level Language ($1000 prize).

Based on the highest performance ranking and a top-ranking in elegance, team kermin (MIT) becomes the winner of the $1,000 award for Higest Performance Design. Because all top-level teams use the same XUP2VP platform, the contest ranking for Most Efficient Design award is identical to the ranking for Highest Performance Design award. However, the contest rules specifically support only a single award should a team win in both categories. The prize for Most Efficient Design can therefore not be awarded to team kermin. The judging panel concluded to award a $500 honorable mention to team vijay, based on the consensus that this design has superior elegance (although this design does not qualify for Highest Performance nor Most Efficient).

The third award, for Best Figures of Merit Using a High Level Language was decided separately under the figures of merit defined by Xilinx, the sponsor of this award. In this category, team kermin was the winner of the $1,000 prize.

The MEMOCODE 2008 Hardware Software Codesign Contest was an exciting event that generated significant outside interest. The contest demonstrated that Hardware Software Codesign remains a challenging topic. The number of finishing teams quadrupled over last year, which opens up the road towards next years' challenge.

Patrick Schaumont. schaum@vt.edu

IEEE Council on EDA's Distinguished Speaker Lecture and Reception

Tuesday, June 10, 12:00pm - 2:00pm Rm: 303AB

The IEEE Council on Electronic Design Automation (CEDA) is holding a lunch to honor Prof. Robert Brayton, the winner of the 2007 Phil Kaufman Award, for his demonstrable impact on the field of electronic design through contributions in Electronic Design Automation (EDA). Prof. Brayton will deliver an inspirational talk, highlighting his career path and challenges, shedding light on turning points while in industry and in academia. In addition to this lecture, EDA award recipients (e.g., IEEE Fellow, IEEE Technical Field Awards, etc.) will be recognized for their accomplishments during the luncheon. The first 125 attendees will receive free lunch. There will be standing room for all others.

IEEE Annual Honors Ceremony

The annual Honors Ceremony, considered to be IEEE's most prestigious event, recognizes exceptional contributions that have made a lasting impact on technology, society and the engineering profession. The program honors achievements in industry, research, education and service. There will be 17 Institute-level award recipients recognized at the 2008 IEEE Honors Ceremony.

The event will be hosted by the 2008 IEEE President and CEO, Lewis Terman. The theme for the IEEE Honors Ceremony will be "Innovating to Meet the World's Challenges."

This year's IEEE Honors Ceremony will be held on Saturday, 20 September 2008, in conjunction with IEEE Sections Congress at the Quebec City Convention Center, Quebec, Canada. The ceremony is planned to start at 6:00pm that evening, with a dinner and afterglow reception immediately following the conclusion of the ceremony.

All those attending Sections Congress are invited to the IEEE Honors Ceremony, dinner and afterglow reception.

For further information, please visit the "Awards News" in the IEEE website.

Networks-on-Chips and EDA Tools to Improve Energy-Efficiency of MPSoC Designs

Reported by Prof. Srinivasan Murali (EPFL, Switzerland)

Several MPSoCs are used in many devices, where a low energy operation of the system is critical. As technology avances, wire scaling is not on par with transistor scaling. This, coupled with the fact that the number of communicating components in the chip and their speed of operation is increasing, has lead to the scenario where the communication between the cores is a major bottleneck for system performance and energy consumption. With architectures being more interconnect dominated, achieving an energy efficient on-chip interconnect architecture, tailored to the needs of the applications running on the chip is an important challenge faced by the designers.

In recent years, researchers have been addressing this challenge in two ways: by developing methods and CAD tools to achieve an energy-efficient design and by developing scalable micro-network based architectures (NoCs). CAD tools allow an exploration of the interconnect design space early in the design cycle and automate the building of efficient application-specific interconnect architectures. The NoC paradigm results in structured, modular interconnect design with improved performance and energy efficiency.

The main goal is to allow designers to explore trade-offs in interconnect design, e.g. between bandwidth, power, reliability, area cost. State-of-the-art methods do exist to solve some of the most important and time-intensive problems encountered during interconnect design, such as interconnect topology synthesis, core mapping, crossbar sizing, route generation, resource reservation, RTL code and layout generation. Application specific interconnect optimization can lead very significant improvements in all relevant cost metrics. Factors of 2 to 5 im-

provements are not uncommon, and become even more significant with technology and architectural complexity scaling. Design automation support is essential to guarantee that these custom-fit solutions can be readily deployed, tested and verified. Even though the state of maturity of these tools is not perfect, results are promising, and automated interconnect design is poised to become an essential component in energy aware SoC design and validation flows.

In this regard, to have fewer design re-spins and faster time-to-market, design flows for NoC interconnects need to integrate the architectural models with back-end physical design models, thereby bridging a big design gap in NoC synthesis and creating on-chip interconnects free from deadlocks. Moreover, to handle the wiring complexity issue in NoC synthesis, accurate estimations of the interconnect delay and power consumption of the basic building blocks of NoCs early in the design phase are key to produce suitable interconnects for latest MPSoCs. Custom NoC topology design, where a NoC is tailored to fit the target application, has noticeable potential benefits with respect to regular topologies, such as, mesh-based NoCs. All in all, the current NoC architectural blocks and design flows for custom NoC topology design have reached a level of maturity comparable to traditional bus-based on-chip interconnects.

Several research directions still exist to make feasible efficient designs of NoC interconnects for new nano-scale devices and technologies. First, efficient support at the NoCs level to handle blocks of MPSoCs working at different operating frequencies or GALS is still an open question. Also, mechanisms for NoC partitioning to provide QoS for new downloaded applications is a very challenging problem. Additionally, the possible benefits of applying runtime dynamic control to NoCs (e.g., dynamic routing schemes) to improve statically partitioned MPSoCs at compile time is an open question. All these extensions to current NoC designs would require changes in both the synthesis algorithm and architectural implementations. Finally, a novel and very interesting research avenue is the design of 3D NoCs, which target next-generation stacked chips. In this regard, according to the yield and speed of vertical interconnects, many different NoC architectures and topologies can be envisioned, as well as the possible inclusion of various fault tolerant schemes, and the definition of suitable choices for each case are still to be explored. Moreover, the CAD support in this case would become even more critical and we expect a large set of new research challenges for NoC design in this area.

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Upcoming Conferences */ Bill Joyner, william.joyner@src.org*

MPSoC	Aachen (Germany), June 23-27, 2008
PATMOS	Lisbon (Portugal), Sept. 10-12, 2008
Nano-Net	Boston (USA), Sept. 15-17, 2008
VLSI-SOC	Rhodes (Greece), Oct. 13-15, 2008
ESWEEK	Atlanta (USA), Oct. 19-24, 2008
FMCAD	Portland (USA), November, 2008
ICCAD	San Jose (USA), Nov. 10-13, 2008

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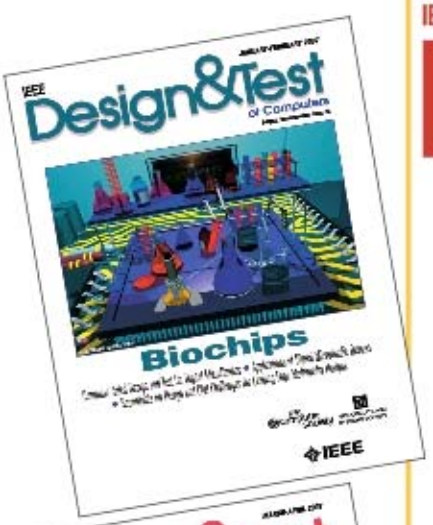

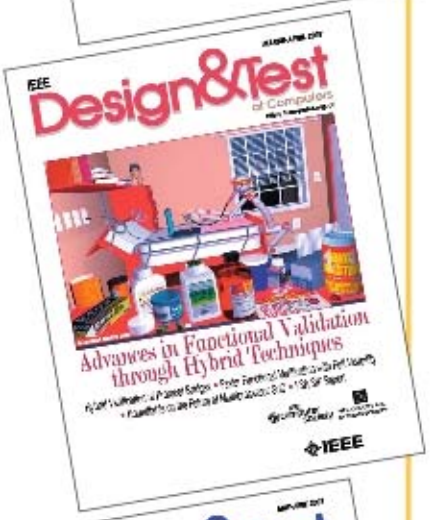

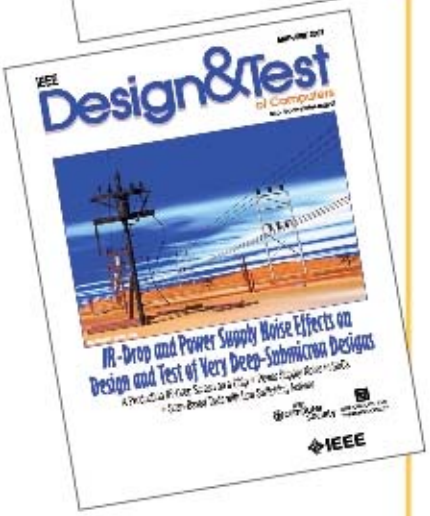

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