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Kaufman award honors Brayton

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PORTLAND, Ore. — Design automation pioneer Robert Brayton is to receive the Nobel Prize of the EDA Industry--the Phil Kaufman Award 2007. Brayton is credited with seminal contributions to the fundamental design automation algorithms used to fabricate integrated circuits, ranging from logic synthesis to the silicon compiler.

"My early work on logic synthesis is what I am best known for, but today I'm interested in its commonality with formal verification methods, too," said Brayton. "Today, I am looking at how these two areas are synergistic with each other--enabling cross-fertilization by borrowing techniques from one to use in the other."

Brayton's latest cross-fertilization ideas will be featured in his keynote speech at this fall's FMCAD (Nov. 11"14, Austin, Texas) where he will address these issues in his talk entitled, "The synergy between logic synthesis and equivalence checking."

The EDA Consortium and the IEEE Council on EDA will formally present the Kaufman award to Brayton two weeks earlier, on Nov. 1, at the 14th annual Phil Kaufman Award ceremony in Santa Clara, Calif.

The award was established in 1994 by the EDA Consortium and the IEEE Council on EDA to honor Phil Kaufman—the late president of Quickturn Design Systems Inc., which merged with Cadence Design Systems Inc. in 1999. Other design automation pioneers who have received the award include Carver Mead, Hermann Gummel, Donald Pederson, James Solomon and Alberto Sangiovanni-Vincentelli, co-founder of Cadence Design Systems and Synopsys.

Brayton studied electrical engineering at Iowa State University (Ames), but he wanted to apply computers to his EE work. At the time, computers were the domain of the mathematics department, so he took his Ph.D. in mathematics from the Massachusetts Institute of Technology (Cambridge).

"I entered MIT in the 1960s with an interest in computers, but at that time the only way to do logic on computers was in the mathematics department. I combined the two disciplines after I entered IBM," Brayton said.

Tenure with IBM

Brayton was hired by IBM's Thomas J. Watson Research Center in Yorktown Heights, N.Y., immediately after graduating from MIT in 1961, and stayed at IBM for 26 years. He began his second career as a professor at the University of California (Berkeley) in 1987, where he has remained for 20 years.

Brayton's seminal work at IBM began with its general-purpose analog circuit simulator—a precursor to the open-source SPICE program developed at his future home after IBM, UC Berkeley. Since then, derivatives of these early logic synthesis efforts have been mimicked by every major EDA programming staff, including HSPICE (by Synopsys) and PSPICE (by Cadence Design Systems), and XSPICE (by Georgia Tech, which added mixed signal code models).

The logic synthesis algorithms to which Brayton made major contributions include the "sparse tableau" and "backward differentiation" methods. These combine the tableau approach with formulas that automate network design optimization using time-step numerical integration--repeatedly solving linear algebraic equations for a sparse matrix.

"I also co-developed a program called Expresso, which was a two-level logic optimization program that became used throughout the industry," he said. "A lot of the logic synthesis companies today still use something like Expresso under the covers."

Brayton also was a pioneer in combining logic-synthesis with place-and-route algorithms during the development of the Yorktown Silicon Compiler at IBM. This seminal project transformed a circuit's behavioral description into a design implementation in terms of logic gates.

"The Yorktown Silicon Compiler, which I developed with Alberto Sangiovanni, demonstrated a particular way of combining logic-synthesis with place-and-route [algorithms] that the whole industry has made many variations on since," said Brayton.

Shortly after working on the Yorktown Silicon Complier, Brayton joined the group at UC Berkeley that developed Spice. Since then the whole CAD and EDA software world has built upon the principles employed in these seminal efforts.

"The EDA world is far beyond what we did with logic synthesis and the silicon compiler," said Brayton. "Today they have to worry about crosstalk, and worry about power, and worry about [the effects of] sizing."

Design challenges

Today Brayton is also working on these problems at the forefront of design automation, particularly on the verification algorithms that are needed to ensure that chips designed for the advanced semiconductor nodes have high yields.

"The work of design automation is getting harder and harder," said Brayton. "There is a greater need for more innovative solutions than we have ever had before. The shrinking [to advanced nodes] creates so many problems in designing chips that they need to be verified--that today verification is essential to getting chips to work properly."

According to Brayton, these greater design automation problems also present greater opportunities for students to enjoy a fruitful and lucrative career while working on interesting problems that are increasingly important.

"My students keep getting job offers that tempt them to leave before even finishing their Ph.D.'s," said Brayton. "The kind of training they are receiving by working on these challenging problems—developing algorithms that attack huge problems—qualifies them in a variety of other areas too, such as for financial applications."

Brayton is an IEEE Fellow, a member of the National Academy of Engineering, and has already received the IEEE Circuits and Systems Technical Achievement Award, the Circuits and Systems Golden Jubilee Award, the IEEE Millennium Medal, the Emanuel R. Piore Award,'the Iowa State University Marston Medal, the European Design Automation Society lifetime achievement award and the ACM Paris Kanellakis Theory and Practice Award.