CALL FOR PARTICIPATION: EDPS 2018

In this annual gathering of electronic IC/system designers and developers, we will discuss design methodologies, design flows and CAD tool needs via presentations or panel discussions.

For 2018, we are seeking presenters in the following areas:

- Cyber Systems Design with emphasis on security
- Machine Learning in System Design and EDA
- Smart Manufacturing; Increased cooperation between design and manufacturing, Advanced Packaging, IoT, Machine Learning, Cloud manufacturing, Supply Chain Safety
- Innovative Designs and Design Techniques (incl. validation and debug)
- System reliability with special focus on ADAS and 5G

Please contact Shishpal Rawat (ssrawat@iitkalumni.org) to submit abstract and discuss areas of mutual interest. All presentations slides must be made available in final form by Aug 15, 2018.

About EDPS:

The 2018 Electronic Design Process Symposium is the leading forum for advanced chip and systems development and CAD methodologies.

As we approach the end of Moore's law scaling, innovative packaging techniques are becoming increasingly important as package, board and other system components drive significant cost reduction. Innovative and smart manufacturing methodologies and flows are also becoming increasingly important. Since algorithmic development is changing rapidly, smart manufacturing enabling reduced NRE and faster time to market is critical.

Among other things, datacenter applications require heightened cybersecurity. 3DIC chip stacking of host processor and accelerator avoids exposing the bus between them to cyber-attacks. Implementation of machine and deep learning algorithms provides a higher level of defense against hacking. Cybersecurity is also very critical in system designs such as the ones found in automotive applications.

Reliability at the system level as well as at the package and chip level is impacted by ESD and thermal issues. Guaranteed performance needs to take aging and power into account. Newer interconnect, changing communication protocols and wide range of operating conditions for systems require enhanced reliability for power and signal interconnects.

Heterogeneous integration of chips in high-performance processes and chips in mature process nodes allows higher performance and better yield optimization. More flexible system level partitioning will lead the way to new products' development. Architectural modularity and IP re-use will enable higher performance at lower total system cost. New FPGA methodologies, especially embedded FPGA will see extensive use.

And last but not the least, machine learning is permeating all fields of system design and design tools.