IEEE Design&Test

Call for Contributions

Special Issue on "Hardware Accelerators for Data Centers"

Data centers around the world have been expanding and multiplying rapidly in the last decade with increased Internet use, online services, compute consolidation, and data analytics. The Natural Resources Defense Council (NRDC) reports that data centers are among the fastest growing consumers of electricity in the developed world. Hardware accelerators are being considered as important architectural components in the context of data center customization to achieve high performance and low energy. Prominent companies have introduced FPGA/GPU-based platforms for data centers. For example, IBM's Coherent Accelerator Processor Interface (CAPI) and Intel's Quick-Assist Accelerator Abstraction Layer enable integration of CPUs and FPGAs/GPUs through coherent shared memory. Microsoft built the Catapult FPGA platform for data centers and demonstrated significant performance improvements for the Bing search. In addition to FPGAs/GPUs, application-specific hardware accelerators are being integrated into platforms for widely-used workloads such as compression, cryptography, and pattern matching. Google's "Tensor Processing Unit" is reported to be used to accelerate machine learning workloads at Google's data centers.

This special issue solicits transformative ideas related to the design and test of energy efficient, high performance and secure data center architectures via hardware accelerators. **Topics of interest include, but are not limited to:**

(1) Accelerator design for important current, emerging, and novel data center workloads (e.g. database, big data, internet of things, machine learning, visual/speech recognition, video, bioinformatics).
(2) Accelerator design for infrastructure (e.g. networking, storage, memory, security, telemetry).
(3) FPGA/GPU based accelerators in the data center (where, how, and why)
(4) Systems management, virtualization, security, and reliability of accelerators in the data center
(5) Programming frameworks and programming models for accelerators in the data center
(6) Performance, energy, and thermal trade-offs of heterogeneous compute in the data center
(7) Design, test, and debug techniques for accelerator-rich heterogeneous data centers

Submission Guidelines:
Guidelines for IEEE D&T papers are given at: http://ieee-ceda.org/publications/d-t/paper-submission

Please choose the special session category "HardwareAccelerators-SI" while submitting the manuscript to the ScholarOne Manuscripts website (https://mc.manuscriptcentral.com/dandt).

Paper Submission and Review Schedule:	
Submission Deadline:	19 Dec 2016
Notification of First Round:	30 Jan 2017
Submission of Revisions:	27 Feb 2017
Final Notification:	3 Apr 2017
Final Paper Due:	1 May 2017

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