IEEE Design & Test

IEEE Design & Test Special Issue Call for Papers

"The Challenges and Opportunities in Analog/Mixed-signal CAD"

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With the advent of "Internet of Things", always connected, sensor driven electronics are becoming a pervasive part of our lives. Fueled by the commoditization of digital compute capabilities, open source hardware movement such as Arduino, and the relentless advances in biomedical electronics, this trend is only going to accelerate. Yet despite the digital processing that is at the core of such electronics, the environment in which these devices operate is inherently analog. We refer to any system that combines analog and associated digital circuitry on the same chip as a mixed-signal system. For instance, the thermal control in a chip, although digital, relies on temperature sensors and pre-processing that is analog. Similarly, the transmission of digital data at high speeds of over 20GB/sec from one chip to the other via protocols such as PCIe, DDR etc. have to transmit data over a physical medium that is analog. Considerable analog processing happens at the transmitter and the receiver in terms of equalization to compensate for channel losses and in clock data circuits in when the transmit clock is not forwarded. Even in a purely digital context, there are many clock domains in a modern day CPU and each requires a PLL, which generates these clocks from a master crystal clock. Similarly, for power considerations, the CPU is divided into several voltage domains with each domain needing a robust supply voltage that can be turned on and off seamlessly. This requires voltage regulators which can supply constant voltages even when there are surges in load current as a voltage domain is turned on. Finally, the analog signals from the environment need to be converted to digital form using sampling and quantization for digital processing and at the other end converted back to analog through interpolation to send the output back to the environment.

As a result, the analog mixed-signal, AMS for short, circuits are occupying an increasingly large percentage of the die area. What makes them especially challenging is that the analog portion of these AMS circuits do not get all the benefits of technology scaling and are more susceptible to variations inherent in smaller feature size nodes. Therefore, variation compensation implemented as a digital control is often an integral part of such circuits. CAD tools are key enablers for successful completion of such AMS circuits and to prevent silicon respins. Unfortunately, analog CAD tools are not as mature as the digital design CAD tools. To foster active research in analog CAD, *IEEE Design and Test* solicits papers in this area. The topics include but are not limited to:

1) Accurate and fast simulations of analog-mixed signal circuits
2) Behavioral modeling and System level analysis

3) Mixed-signal control loop verifications in PLLs, High-speed IOs and Voltage regulators
4) Variation and yield centering
5) Formal verification of analog circuits
6) Analog synthesis
7) Early layout effects modeling in design
8) Noise and reliability effects in analog systems
9) Analog test and post-silicon debug

Submission and Review Process

Prospective authors should follow the submission guidelines for IEEE Design & Test. All manuscripts must be submitted electronically to the IEEE Manuscript Central Web site at https://mc.manuscriptcentral.com/cs-ieee. Indicate that you are submitting your article to the special issue on ''The Challenges and Opportunities in Analog/Mixed-signal CAD''. All articles will undergo the standard *IEEE Design & Test* review process. Submitted manuscripts must not have been previously published or currently submitted for publication elsewhere. Accepted articles will be edited for clarity, structure, readability, and grammar. Please see *IEEE Design & Test* website for detailed author guidelines.

Key Dates

- **Articles due for review: 15th December, 2015**
- **Reviews completed: 15th February, 2016**
- **Article revisions due: 15th March, 2016**
- **Notice of final acceptance: 15th April, 2016**
- **All materials due to edit: 15th May, 2016**
- **Publication date: July/August 2016**

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