IEEE Design&Test

Call for Contributions

Special Issue on "Emerging Challenges and Solutions in SoC Verification"

Verification has been one of the major bottlenecks in integrated circuit design process, which is exacerbated by the sheering design complexities nowadays. The increased design size is only one dimension of the growing complexities. Recent System-on-Chips (SoC) often feature multiple heterogeneous embedded processors and accelerators. While the heterogeneous architecture is more power efficient, it adds verification complexities of the hardware/software interaction and interconnect coherency. It is common that tens or hundreds of IP blocks, among which analog IPs occupy an increasing portion, are integrated into a single chip. Moreover, the growing market shares of devices for Internet-of-Things (IoT) and automotive applications have signified the requirements for verifying security and safety, which adds new dimensions to the complexities. As a result, the industry has encountered emerging challenges for correctly verifying increasingly complex SoCs in a timely manner, which create the "verification gap". Numerous resources in the industry and academia has been devoted to addressing the verification challenges, the needs for advanced verification technologies to close the gap, and state-of-the-art solutions.

The objective of this special issue is to provide a forum for academic and industry researchers to publish new research results that solve the outstanding challenges associated with complex SOC Verification. Survey papers of the state of the art solutions are also encouraged.

Topics of interest include, but are not limited to:

1. Stimulus Generation and Reuse: Simulation-based verification quality relies on generating stimulus to exercise the design thoroughly to achieve coverage closure efficiently and to enable reuse at different stages of verification.
2. Emulation and FPGA Prototyping: Growing adoption of simulation acceleration technologies such as emulation and FPGA prototyping. Challenges in model creation, testbench migration and debug enablement.
3. ESL Verification and Virtual Platforms: The complexities of software/hardware interactions require that software validation start at an early stage of the design process prior to RTL availability creating the need for virtual platforms.
4. Post-Silicon Validation: Post-silicon validation is still very important in capturing bugs escaping pre-silicon verification. Reuse of verification collateral and debugging under limited observability remain challenging.
5. Triage and Debug Automation: Debug remains a manual effort causing huge bottlenecks. Automation tools to reduce human involvement in triage and debug at all stages of verification are highly desirable.
6. Data Analytics: Extracting knowledge from the large amounts of data generated during verification and often discarded after simplistic analysis.
7. Automatic Formal Verification: Domain-specific applications targeting specific properties can help boost productivity
8. Mixed Signal Verification: Internet of things (IoT) SOC devices contain significant analog and sensor circuitry, hence the need for efficient mixed-signal verification methodologies is increasingly important.
9. Security and Safety Verification: Emerging design requirements such as security and safety add non-linear complexities intertwined with normal functionality, hence, the need for solutions targeting these features.

Submission Guidelines:

Guidelines for IEEE D&T paper are given at: http://ieee-ceda.org/publications/d-t/paper-submission

Please choose the special session category "Verification-SI" while submitting the manuscript to the ScholarOne Manuscripts website (https://mc.manuscriptcentral.com/dandt).

Paper Submission and Review Schedule:

Submission Deadline:	31 October 2016
First Round of Reviews:	19 December 2016
Revisions Due:	16 January 2017
Notification of Final Acceptance:	13 February 2017
Camera Ready Due:	27 February 2017

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