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CEDA

IEEE Council on Electronic Design Automation

Newsletter

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February 2024

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CONFERENCES PUBLICATIONS

ANNOUNCEMENTS CALLBOARD

2024 Outstanding Service Recognition Recipients

CEDA would like to recognize the following volunteers for their exceptional commitment and service to the EDA community as the 2023 General Chair of the five major CEDA conferences.

- Atsushi Takahashi - ASP-DAC
- Ian O'Connor - DATE
- Jörg Henkel - DAC
- X. Sharon Hu - ESWEEK
- Evangeline F. Y. Young - ICCAD

Learn More

IEEE CEDA Ernest S. Kuh Early Career Award

Nomination Deadline: 15 April 2024

The IEEE CEDA Ernest S. Kuh Early Career Award honors an individual who has made innovative and substantial technical contributions to the area of Electronic Design Automation in the early stages of his or her career.

Prize: $1,000 and an engraved plaque.

Presentation: The award will be presented at the 2024 ICCAD conference

Submit a Nomination

DATE 2024 Distinguished Speaker: Helen Li

Each year, CEDA invites experts in EDA to present at the Design, Automation, and Test in Europe (DATE). IEEE CEDA Distinguished Speaker Luncheon will be presented by Hai (Helen) Li, Clare Boothe Luce Professor of Electrical and Computer Engineering at Duke University.

Date: Monday, 25 March 2024
Time: 12:00 PM CET
Location: DATE 2024 in Valencia, Spain

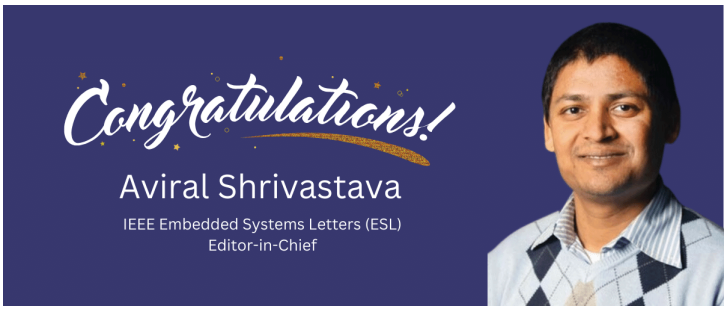
Presenter: Hai (Helen) Li, Clare Boothe Luce Professor of Electrical and Computer Engineering at Duke University.

Talk Title: AI Models for Edge Computing: Hardware-aware Optimizations for Efficiency

Abstract: As artificial intelligence (AI) transforms various industries, state-of-the-art models have exploded in size and capability. The growth in AI model complexity is rapidly outstripping hardware evolution, making the deployment of these models on edge devices remain challenging. To enable advanced AI locally, models must be optimized for fitting into the hardware constraints. In this presentation, we will first discuss how computing hardware designs impact the effectiveness of commonly used AI model optimizations for efficiency, including techniques like quantization and pruning. Additionally, we will present several methods, such as hardware-aware quantization and structured pruning, to demonstrate the significance of software/hardware co-design. We will also demonstrate how these methods can be understood via a straightforward

theoretical framework, facilitating their seamless integration in practical applications and their straightforward extension to distributed edge computing. At the conclusion of our presentation, we will share our insights and vision for achieving efficient and robust AI at the edge.

DATE 2024

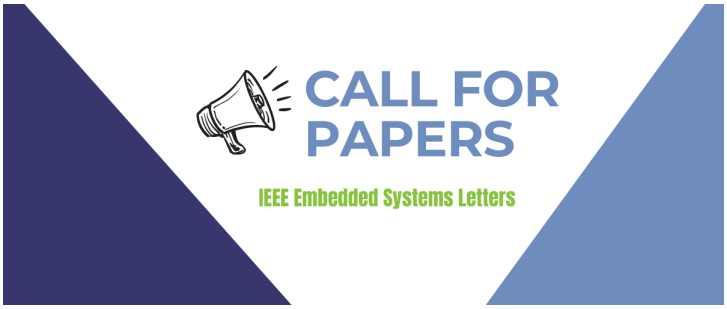


Aviral Shrivastava Appointed Editor-in-Chief for the IEEE Embedded Systems Letters (ESL)

IEEE CEDA would like to congratulate Professor Aviral Shrivastava on this appointment!

Aviral Shrivastava is a full Professor in the School of Computing and Augmented Intelligence (SCAI) at Arizona State University, where he established and heads the **Make Programming Simple Lab**. He completed his Ph.D. in Information and Computer Science and from the University of California, Irvine, and his Bachelor's in Computer Science and Engineering from IIT Delhi.

About ESL



ESL Special Issue Call for Papers

The submission deadline for the Special Issue on "Languages Compilers Tools and Theory of Embedded Systems" is 15 June 2024.

The ACM SIGPLAN/SIGBED Conference on Languages, Compilers, Tools and Theory for Embedded Systems (LCTES 2024) will be held on June 24, 2024 in Copenhagen, Denmark. This special issue in the IEEE Embedded Systems Letters will consider peer-reviewed journal versions of submissions to LCTES 2024, as well as other papers received from the open call that fit within the scope of LCTES.

Embedded system design faces many challenges both with respect to functional requirements and nonfunctional requirements, many of which are conflicting. They are found in areas such as design and developer productivity, verification, validation, maintainability, and meeting performance goals and resource constraints. Novel design-time and run-time approaches are needed to meet the demand of emerging applications and to exploit new hardware paradigms.

Download CFP

JxCDC Special Issue Call for Papers

The submission deadline for the Special Issue on "3D Logic and Memory for Energy Efficient Computing" is 31 May 2024

Monolithic microelectronic design is facing tremendous challenges in the growing need of computation memory bandwidth and latency, and the energy efficiency of computation which is limiting its performance and cost. Although recent advances (e.g., domain-specific acceleration, near-memory and in-memory computing techniques) try to address these issues, the scaling trend of monolithic design still lags behind the ever-increasing demand of AI algorithms, highperformance computing, high-definition sensing and other data-intensive applications. In this context, technological innovations, in particular 3D integration through packaging and monolithic methods, are critical to enabling heterogeneous integration (HI) and bringing significant performance, energy and cost benefits beyond traditional chip design. 3D logic and memory design allow heterogeneous functional macros (i.e. chiplets) to be flexibly produced and connected with higher interconnection density, length reduction and area utilization, opening new opportunities across the microelectronic design stack.

Download CFP

2024-2025 CEDA Distinguished Lecturer Nominations Open

Nomination Deadline: 30 April 2024

The IEEE CEDA Distinguished Lecturer Program promotes the field of electronic design automation to the scientific community and the public at large. The program aims to increase awareness about topics relevant to CEDA by creating a pool of subject matter experts and scholars to present to IEEE and CEDA Chapters, Sections, and other venues such as universities and companies.

Important Information:

- The DL nominee must be nominated by a CEDA participant who does not have a conflict with the selection process.
- No self-nomination is allowed.

- If you are looking for a nominator, we encourage you to contact your local CEDA Chapter Chair.
- The DL nominee must be a well-recognized expert in their field because of their research, teaching, and service activities, and as an inspiring speaker.

Nomination Form

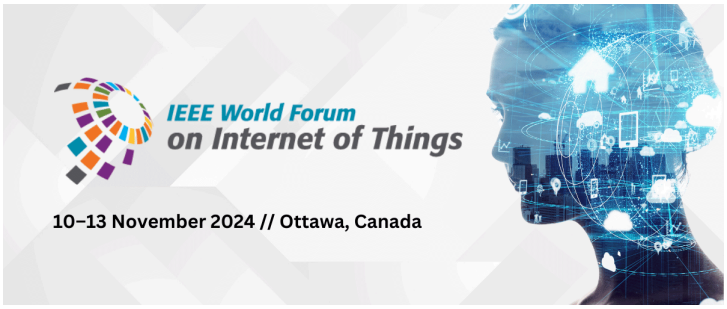
33rd International Workshop on Logic & Synthesis

Deadline to submit abstracts: 29 March 2024

The **International Workshop on Logic and Synthesis** is the premier forum for research in synthesis, optimization, and verification of integrated circuits and systems. Research on logic synthesis for emerging technologies and for novel computing platforms, such as nanoscale systems and biological systems, is also strongly encouraged. The workshop encourages the early dissemination of ideas and results. The workshop accepts complete papers highlighting important new problems in the early stages of development, without providing complete solutions. The emphasis is on novelty and intellectual rigor.

The workshop format includes paper presentations, invited talks, social lunch and dinner gatherings, and recreational activities.

Call for Papers



10th IEEE World Forum on Internet of Things!

Full Paper Submission Deadline: 1 April 2024

The IEEE **WFIoT2024** continues the legacy of being the premier event hosted by the IEEE IoT Technical Community, uniting diverse expertise intrinsic to the IoT domain. This year, we proudly announce the theme for WFIoT 2024: "Unleashing the Power of IoT with AI." This theme underscores the pivotal role of Artificial Intelligence in augmenting the potential of the Internet of Things.

Call for Papers

The First IEEE International Workshop on LLM-Aided Design (LAD'24)

28-29 June 2022 | IBM Research Almaden, San Jose, CA, USA

This new international workshop will focus on how to use LLM (Large Language Model) as a methodology to help design circuits, software, and computing systems with improved quality, productivity, robustness, and cost. It is the first of its kind international workshop in the community that will focus on discussing results that leverage the significant advancement and innovation captured by the generative AI and LLM technology to offer new methods and solutions for design automation targeting various applications. The workshop will be a timely venue that will host leading researchers and thought leaders in this fast-growing area and will provide a forum for researchers and practitioners to present their latest results, contribute open-source LLM models, datasets, tool flows, and offer benchmarking, testing and validation methods and solutions.

Conference Website

Design Automation and Test in Europe (**DATE 2024**)
25-27 March 2024
Valencia, Spain

Design Automation Conference (**DAC 2024**)
23-27 June 2024
San Francisco, CA, USA

Embedded Systems Week (**ESWEEK 2024**)
29 September-4 October 2024
Raleigh, NC, USA

2024 ACM/IEEE International Conference on Computer-Aided Design (**ICCAD 2024**)
Dates TBD
New Jersey, USA

Asia and South Pacific Design Automation Conference (**ASP-DAC 2025**)
20-23 January 2025
TBA, Japan

Contact IEEE CEDA VP of Conferences Tsung-Yi Ho for sponsorship opportunities at **vp.conferences@ieee-ceda.org**.

Publications

IEEE CEDA financially sponsors and co-sponsors several publications and publishes its ***Currents*** newsletter to inform the EDA community on industry news and research results.

Visit the individual publication pages for more information on publication scope, call for papers, and more.

Top Accessed Articles in January 2024 (*as of 26 February 2024)

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems

- **ViA: A Novel Vision-Transformer Accelerator Based on FPGA**
- **Verifying Controllers With Vision-Based Perception Using Safe Approximate Abstractions**
- **TrueNorth: Design and Tool Flow of a 65 mW 1 Million Neuron Programmable Neurosynaptic Chip**

IEEE Design & Test

- **Machine Learning in Advance IC Design: A Methodological Survey**
- **High-Bandwidth Memory (HBM) Test Challenges and Solutions**
- **Testability and Dependability of AI Hardware: Surveys, Trends, Challenges, and Perspectives**

IEEE Embedded Systems Letters

- **Three-Stage Power Supply System Model for a Wearable IoT Device for COVID-19 Patients**
- **Methodology for CNN Implementation in FPGA-Based Embedded Systems**
- **Design of Leading Zero Counters on FPGAs**

Contact IEEE CEDA VP of Publications Jörg Henkel at **henkel@kit.edu** or the journal's respective EiC for questions regarding CEDA-sponsored publications.

Share what's new

We thank you for forwarding this content to others who might be interested including other members of your group or organization.