

IEEE BIT CEDA STUDENT CHAPTER



ACTIVITIES EXECUTED

BANGALORE INSTITUTE OF TECHNOLOGY
K.R Road, V.V pura, Bengaluru - 560004

INAUGURAL CEREMONY
of
IEEE BIT CEDA STUDENT CHAPTER

TECHNICAL TALK ON
Revolutionising Storage: A Deep Dive into 3D NAND Memory

SPEAKER INFORMATION

- Technologist at Western Digital, 10 years in semiconductors.
- Master's in Signal Processing from IIT Kanpur.
- Key roles at Samsung Semiconductor India Research.
- Expert in low-cost, high-bandwidth memory design.
- IEEE Senior Member, 10 patents, 8 trade secrets, 10 technical papers.



Mr. Sajal Mittal

2:00 PM

25-05-2024

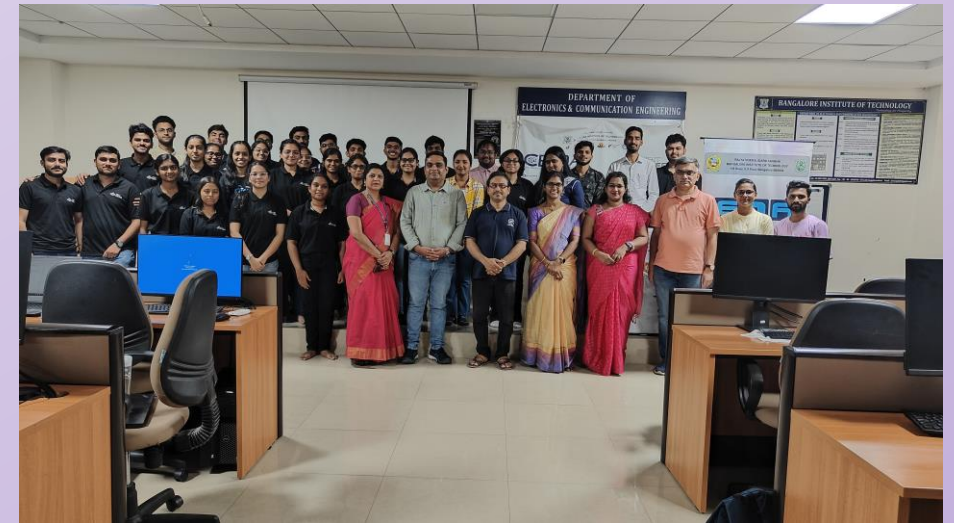
VLSI lab

Mr Alok Das
chief guest

Dr Jalaja S
IEEE BIT SB Counsellor

Dr J Prakash
Vice Principal, BIT

Dr Aswath M U
Principal, BIT



The IEEE BIT CEDA Student Chapter inaugural ceremony featured a technical talk by Mr. Sajal Mittal, a technologist at Western Digital, on the revolutionary 3D NAND memory technology. The event aimed to enlighten attendees on the latest advancements in storage technology and celebrate the beginning of the new student chapter



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IEEE BIT STUDENT BRANCH

in association with

IEEE CEDA STUDENT CHAPTER

presents

VERILOG HDL TEST

FOR

**Compiler design
workshop and project**

Details regarding test is mentioned in Google form



8th June

Contact Info-





Skanda R-8867070040


Dr. Jalaja S
IEEE BIT SB Counsellor

Dr. J Prakash
Vice Principal, BIT

Dr. Aswath M U
Principal, BIT




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COMPILER DESIGN
WORKSHOP

Resource Person
Mr Alok Kumar Das

 **18th & 19th**
June

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IEEE BIT SB Counsellor

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Vice Principal, BIT

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The workshop, organized by EDA Society of IEEE BIT SB, aimed to provide a comprehensive understanding of Verilog compiler design using Lex and Yacc tools. A selective test on Verilog preceded the workshop, with 10 participants chosen to attend the two-day session led by Mr. Alok Das.

ACTIVITIES PLANNED

MONTH	ACTIVITY
JULY	SYSTEM VERILOG WORKSHOP
AUGUST	STEM ACTIVITY
SEPTEMBER	INDUSTRIAL VISIT
OCTOBER	PANEL DISCUSSION
NOVEMBER	TECH TALK ON OPEN SOURCE EDA TOOLS

THANK YOU