IEEE Design&Test

Call for Papers for a Special Issue on

Emerging Challenges with 3D NAND Flash Storage

Aim and Scope

Solid state storage devices offer permanent storage of data and code in a wide range of computing systems found in consumer electronics, automotive, military, industrial, healthcare, and enterprise segments. Non-volatile flash memories, the basic building blocks of solid-state storage devices, offer small form factors, high-capacity, high-speed, and low-power permanent storage solutions. Traditional 2D NAND flash memory technology reached the end of scaling with sub-15 nm technology nodes, hampered by the increasing cost of lithography and deteriorating cell reliability. The industry has responded by shifting to monolithic 3D NAND fabrication processes, opening a new scalability dimension – the number of vertical layers. An increasing number of layers (~232 in the most recent chips) together with continual logical scaling that allows for storing multiple bits per one cell (4 bits can be stored in the most advanced flash memories) promises to extend the current trends towards higher bit density and lower per-bit cost in the next decade. These trends are crucial to meet tremendous demand for data storage solutions. The global 3D NAND flash market size was valued at $12.4 billion in 2020 and is expected to reach $78.4 billion by 2030. This prediction indicates the growing importance of 3D NAND flash memories as the dominant type of technology for storage solutions in years to come. This special issue aims to introduce the design and test community to emerging challenges with 3D NAND Flash storage. It aims to raise awareness of emerging reliability, security, and performance issues with current and emerging Flash technologies and their widespread use. The scope of this special issue spans the entire silicon ecosystem from technology, foundry, design, EDA, test to in-field deployment, and integration into IoT, CPS, edge, and cloud solutions. Through this special issue, we hope to build a cross-disciplinary community of researchers who are motivated by secure, trustworthy, fault-tolerant, high performance, and energy-efficient design and test of storage solutions for emerging computing systems.

Topics of Interest

This special issue is dedicated to the design and test of 3D NAND flash storage in computing systems. It aims to cover diverse aspects of technology, foundry, design, EDA, test to in-field deployment, and integration into IoT, CPS, edge, and cloud solutions. Topics of interest include:

- Computing in/near 3D NAND Flash storage
- Data sanitization issues in 3D NAND Flash storage
- 3D NAND Flash storage for harsh environments
- Sustainable practices for 3D NAND Flash storage
- 3D NAND Flash storage lifecycle management
- Latency enhancements for 3D NAND Flash storage
- Fault-tolerant 3D NAND Flash storage
- Energy-efficient 3D NAND Flash storage
- Resource management for 3D NAND Flash storage
- Security vulnerabilities of 3D NAND Flash storage
- Supply chain security of 3D NAND Flash storage
- 3D NAND Flash for High Performance Computing
- 3D NAND Flash for Embedded and IoT Computing

Submission Guidelines

Prospective authors should follow the submission guidelines for IEEE Design & Test. All manuscripts must be submitted electronically to IEEE Manuscript Central at https://mc.manuscriptcentral.com/dandt. Indicate that you are submitting your article to the *"Special Issue on Emerging Challenges with 3D NAND Flash Storage"*. Manuscripts must not exceed 5,000 words, including figures (with each average-size figure counting as 200 words) and a maximum of 12 references (30 for surveys). This amounts to about 4,000 words of text and a maximum of five small to medium figures. Accepted articles will be edited for clarity, structure, conciseness, grammar, passive to active voice, logical organization, readability, and adherence to style. Please see IEEE Design & Test Author Information at: https://ieee-ceda.org/publication/ieee-design-test-dt/author-info.

Schedule

- Open for submissions : October 1, 2024
- Submission deadline : February 1, 2025
- Notification First Round : April 15, 2025
- Revision submission : April 30, 2025
- Final decisions : June 15, 2025
- Tentative publication : Fall 2025

Guest Editors

Please direct any questions regarding this special issue to one of the following

Sudeep Pasricha, Colorado State University, sudeep@colostate.edu
Biswajit Ray, Colorado State University, biswajit.ray@colostate.edu
Shyam Raghunathan, Micron Technology, Singapore, shyamsunderr@micron.com