CEDA EC Meeting

27 October 2024

Agenda

- Roll Call
- Approval of September Minutes
- Approval of October Agenda
- President’s Welcome and Update
- Finance
- Education and Engagement Activity
- Publications
- Awards
- 20th Anniversary
- Strategy
- Initiatives
- Standards
- Young Professionals
- Publicity
- Conferences
- Technical Activities
- Unfinished Business
- Administrative Updates

Welcome - Silveira

- Roll Call
- Approval of September Minutes
- Approval of October Agenda
- President’s Report

CEDA Fellows Search Committee

IEEE Board recommendations to Fellows Program

- Societies/Councils (S/C) with more than 15 Fellow nominations averaged over the previous 3 cycles shall establish an S/C-FSC.
- The S/C-FSCs are tasked with identifying suitable nominees for possible elevation to IEEE Fellow, with particular emphasis on nominees who reflect the diversity of IEEE and its professional communities.

- CEDA had an average of 15 or more nominations in the previous three Fellow nomination cycles and will need to establish a Fellow Search Committee for the upcoming Fellow nomination cycle (Class of 2026).

IEEE Board recommendations to Fellows Program

- S/C-FSC shall consist of at least seven (7) and up to eleven (11) members appointed by the S/C's AdCom or BoG.
- Members shall be IEEE Fellows who reflect the diverse and global nature of the S/C community
- Appointments are for one-year terms with eligible reappointment for up to two additional terms.

CEDA Fellows Search Committee

- Yao-Wen Chang (R10) <u>Committee Chair</u>
- Valeria Bertacco (R4)
- Krishnendu Chakrabarty (R6)
- Kiyoung Choi (R10)
- Joerg Henkel (R8)
- Sharon Hu (R4)
- Frank Liu (R3)
- Enrico Macii (R8)

CEDA Kaufman Award Dinner

CEDA Table set up

- Gi-Joon Nam
- Deming Chen
- Subhsish Mitra
- Tom Coughlin, IEEE President
- Yao-Wen Chang
- Antun Domic, Kepler Computing
- Kurt Keutzer, UC Berkeley
- Luca Benini, ETH Zurich & U Bologna
- Yong Liu, Cadence
- Frank Schirrmeister, Synopsys

CEDA 20th Anniversary Plans

Status of Preparation

- ”Best of Webpage”
  - Elena-Ioana will lead process, set up team
  - Report at December meeting with a plan
- Video Snapshots/Interviews
  - Georges will report
- Panels @flagship conferences
  - Subasish will report
  - ASP-DAC preparations
- Trivia contest
  - Need volunteers!!

Celebration at DAC

Need to discuss what to do (if anything)

- Anticipated costs of Sunday and Tuesday receptions for DAC 2025
  - Sunday – anticipated spend for 826 attendees: ***$56,672***
  - Tuesday – anticipated spend for 1,271 attendees: ***$86,816.15***

- CEDA could look to add more or swap to a more elevated menu item
  - Sunday:
    - Switching one of the three passed apps to a hearty item: adding $6,021 to current budget
    - Add an additional station or noodle bar / anticipate adding $21,000 to the budget
  - Tuesday:
    - Switching one of the three passed apps to a hearty item: adding $9,300 to current budget
    - Add an additional station or noodle bar / anticipate adding $33,000 to the budget

Finance

Marina Zapater

Oct 27th 2024

Finances 2024 Status (Sept.'24)

- Numbers ramping-up to pre-COVID levels
- Still underspending in many categories
- In others, we will surpass
  (will be compensated)

Cost Centers	Total Expense				
	Annual Budget	YTD Budget	YTD Actual	YTD Marina	
10125-Technical Committee	33'000.00	24'750.00	0.00	0.00	?? --> Same issue than 2023 (careful for 2025)
10130-Education Committee	41'000.00	30'750.00	12'825.24	12'825.24	underspending but ok
10140-Awards Committee	27'500.00	20'625.00	4'227.48	4'227.48	underspending but ok
10155-Chapter Committee	0.00	0.00	21'530.00	21'530.00	ok! (solved 2023 issues)
10180-Conference Committee	55'900.00	41'925.00	39'917.22	39'917.22	ok!
21015-Societies Operations	470'608.61	353'743.31	355'129.61	355'129.61	we will surpass, but will be compensated
21020-Meetings /Conference	22'681.21	14'001.05	18'202.72	18'202.72	
21030-Soc Publication Related Support	67'000.00	28'687.36	32'955.54	32'955.54	slightly surpassed, but ok
Total Cost Center	717'689.82	514'481.72	484'787.81	484'787.81	
Total From Operations	3'906'141.87	3'374'270.09	3'080'076.40	3'080'076.40	
21065-Society Initiatives	67'058.00	50'293.50	27'265.98	35'000.00	Travel grants really ok! Others... not so ok...
21065 Drill-in (travel grants only)				25'000.00	YPP @ DATE (10k), others travel grants
Grand Total	3'973'199.87	3'424'563.59	3'107'342.38	3'107'342.38	

Comparison wrt last year

- Underspending in all categories, except in volunteer travel and contests
- Initiatives being very low
  - Only travel grants (~13k)

210440-Council on Electronic Design Automation

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Budget 2025 – Based on 2024 forecast

- First-pass budget was “submitted” to IEEE in August with items discussed in July EC/BoG meeting
  - Overall, the 2025 budget is based on 2024 forecast, so more or less ok for each specific item, and ok overall.

Other topics

- Careful! Try to submit your expense reports ASAP
  - ICCAD often goes to next year

- The IEEE reimbursement pipeline is being a bit slow these days

Electronics Design for Youngsters

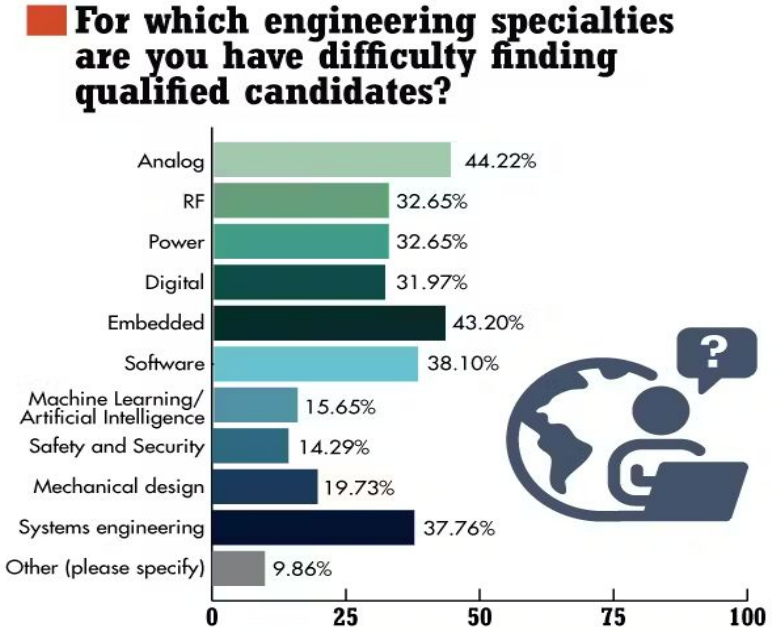
An IEEE CEDA Education Initiative

Cristiana Bolchini, Enrico Macii

October 27, 2024

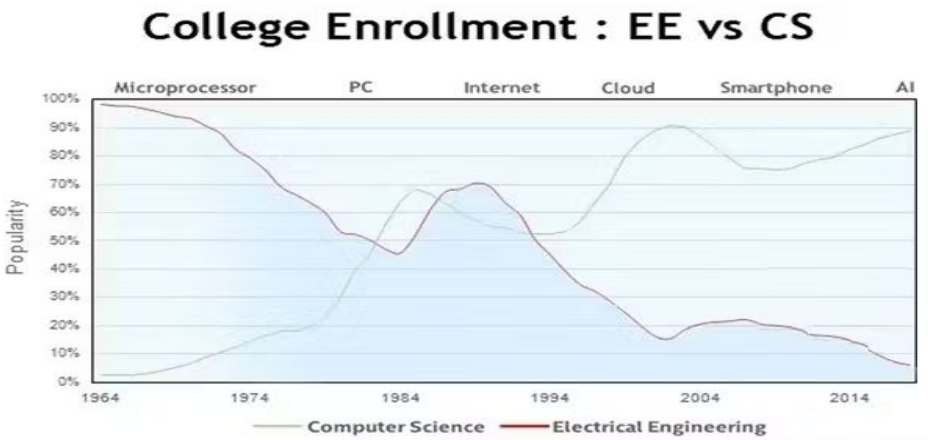
Shortage of design skills

- Semiconductor industry needs hundreds of thousands of new employees
  - 1M new hirings by 2030
    [2023 Semiconductor Industry Outlook by Deloitte]
- Circuits and systems designers are the most critical human resources to be found.



EE vocational crisis

- The world is facing an electronics “vocational” crisis.
- In the ICT domain, “electronics” is not as appealing as other subjects (e.g., AI, Data Science, Cloud, IoT).
  - Interest in EE curricula is steadily declining.



CEDA's initiative

- Develop an educational program to introduce high-school students to electronics design
- Timeline
  - Phase 1: Program set-up (Nov 2023 - Sep 2024)
  - Phase 2: Pilot implementation (Oct 2024 – Mar 2025)
  - Phase 3: Assessment and improvement (Apr 2025 – Jul 2025)
  - Phase 4: World-wide delivery (Aug 2025 on-ward)

Phase 1 - Completed

- The team:
  - Cristiana Bolchini, Fabrizio Ferrandi, POLIMI
  - Enrico Macii, Daniele Jahier Pagliari, Gianvito Urgese, POLITO
- Achievements:
  - Definition of course organization and contents
  - *Identification of design tools and case study, acquisition of FPGA boards*
  - *Development of course and lab material (help from a graduate student)*
  - Identification of 3 high-schools in Italy to host pilot delivery of the course

Phase 2 - In progress

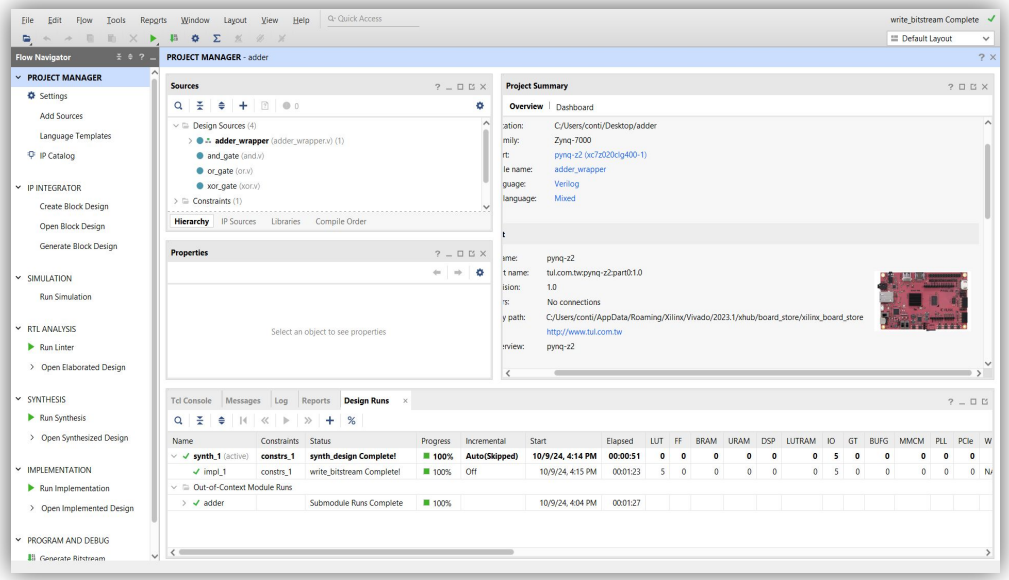
- First pilot edition of the course
  - Where: Torino, Liceo Scientifico Galielo Ferraris
  - When: November 13, 2024-December 16, 2024
  - Organization:
    - 6 lectures of 2 hours each
    - 4 labs of 3 hours each
  - Students:
    - Up to 50 from 4^{th} and 5^{th} year.
  - Location:
    - Politecnico’s classrooms and labs to introduce students to university life

Course and lab contents

1. Electronic Systems and SoC Basics
2. Digital Logic Fundamentals
3. Introduction to EDA
   - Lab 1: Introduction to Vivado and the Design of Simple Logic Gates
   - Lab 2: Adder Design (Design, Simulation, Implementation on Pynq FPGA)
4. SoC Architecture & Design
   - Lab 3: SoC Design (ADC + Timer + GPIO + SW, Implementation on Pynq FPGA)
5. SoC Simulation & Verification
6. Industry testimonial: A Designer from STMicroelectronics shares his experience
   - Lab 4: Design of an SoC capable implementing a NN for “Digit Recognition“

Overview of Lab Sessions

Design Software

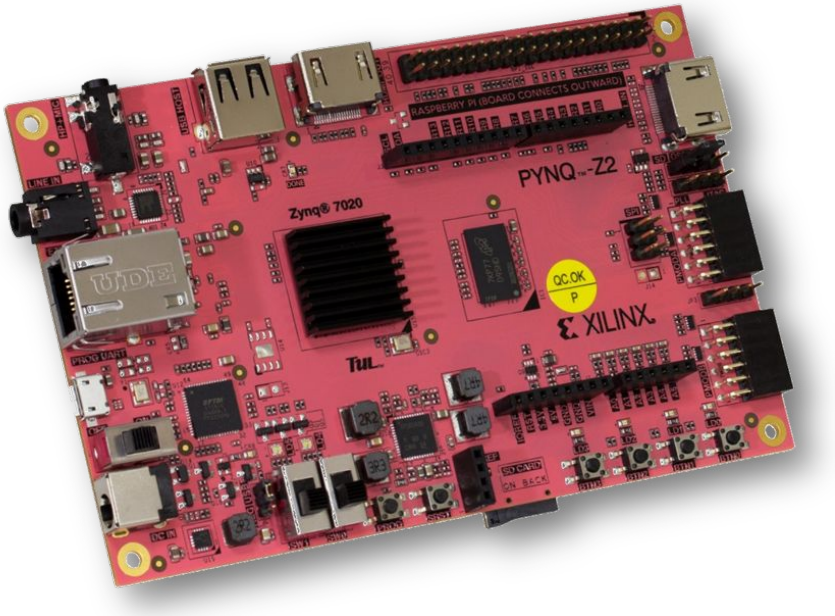


AMD XILINX Vivado 2023.1:

- Synthesis & analysis of HDLs
- Block design integration
- Included logic simulator
- GUI-based commands
- Each laboratory session is prepared as a stand-alone project

AMD XILINX

Development Board

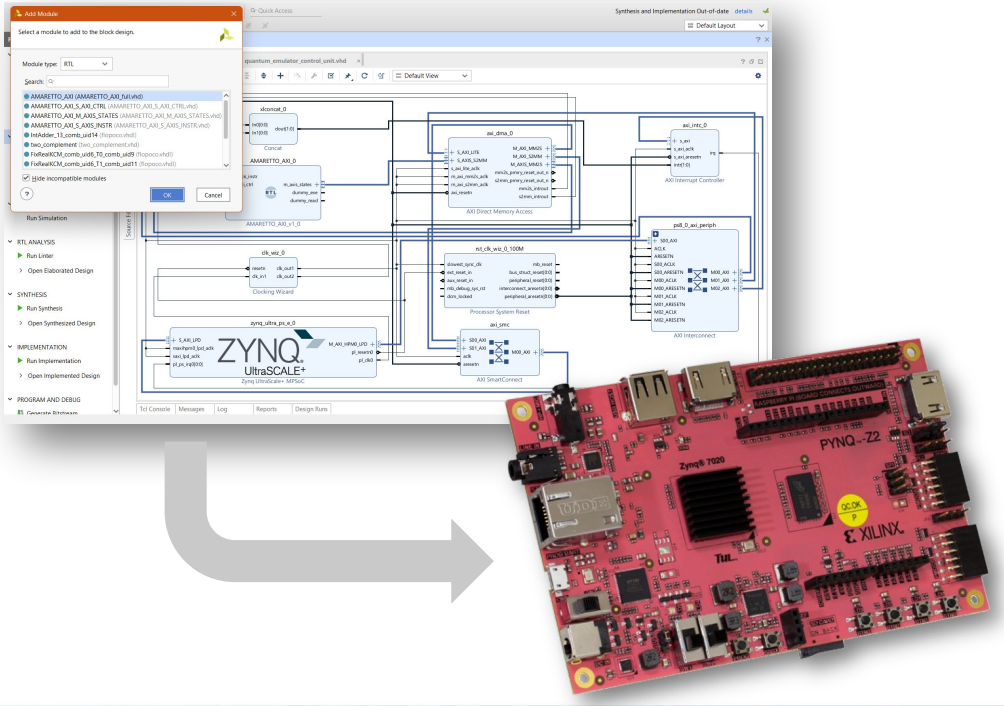


Tul PYNQ-Z2:

- Dual Core ARM core + FPGA
- 4 Buttons
- 4 Green LEDs
- 2 Switches
- 2 High intensity RGB LEDs
- Running on PYNQ Overlays (FPGA interface in Python)

AMD XILINX

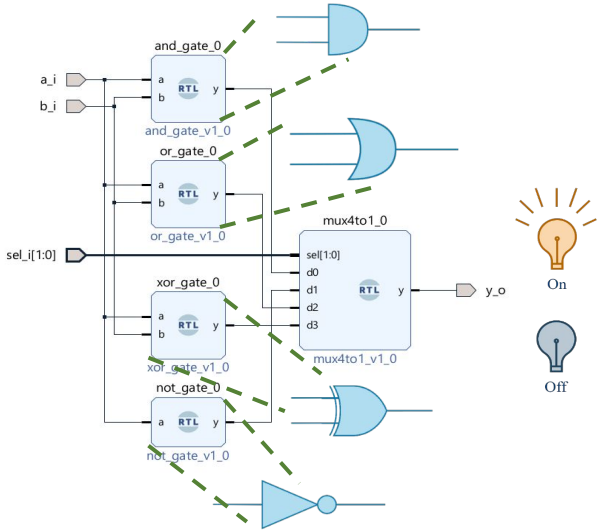
Students Activities



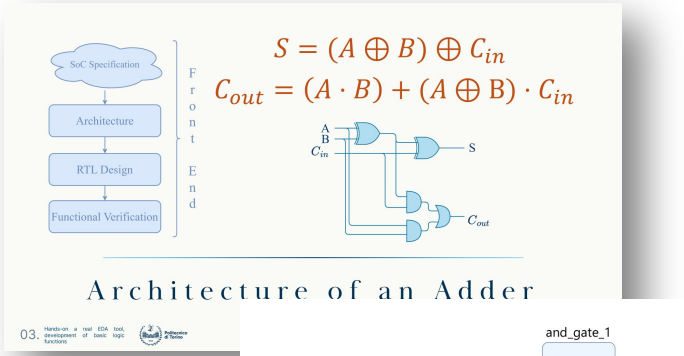
- Laboratories will gradually increase in complexity
- From a “pencil & paper” approach to a real implementation with the help of an EDA tool
- Block Design and interconnections between functional blocks as students' entry point

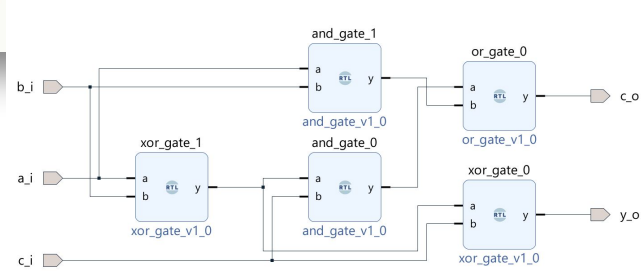
Lab 1: Logic Gates

- Introduction to Vivado
- Getting familiar with Block Design, interconnections, and logic simulation
- Implementation of basic logic gates, a multiplexer, and deployment on the board



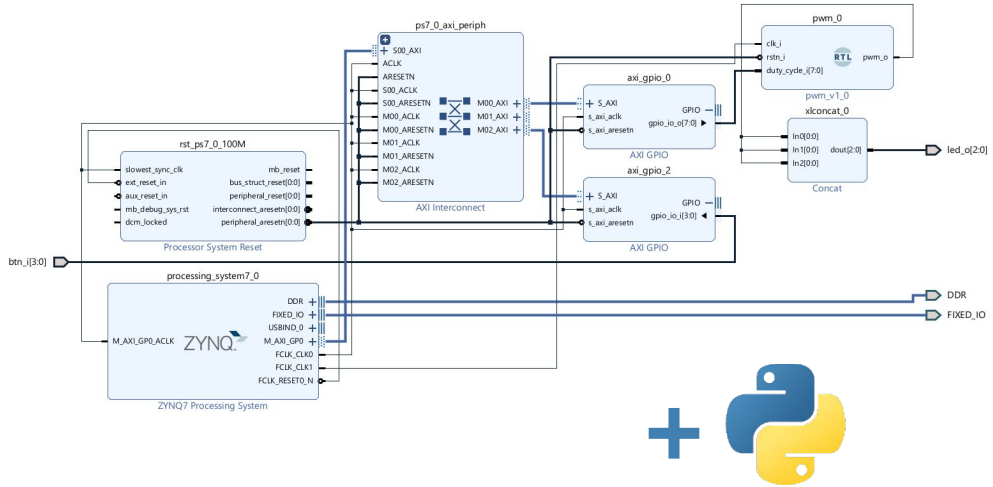
Lab 2: Full Adder





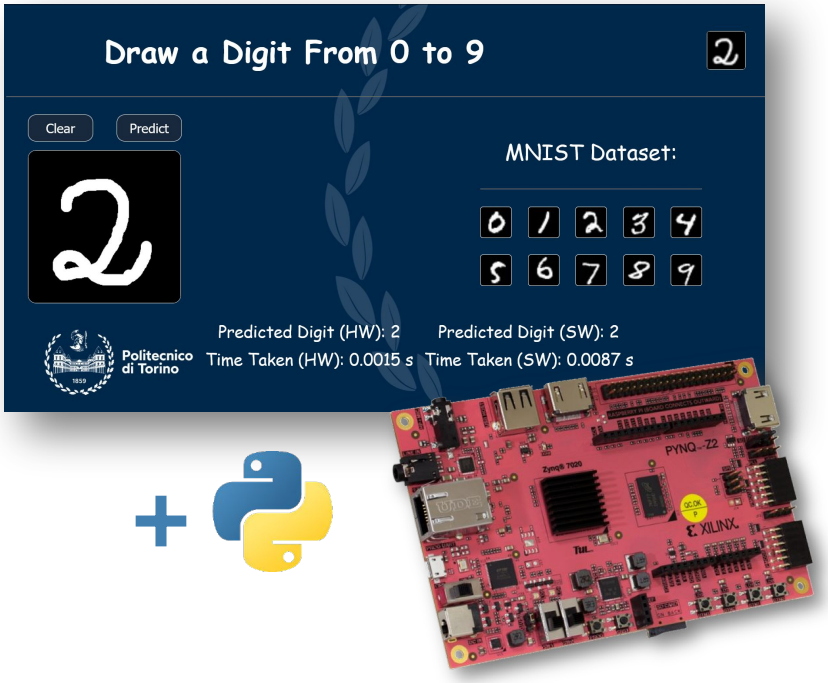
- Design of a simple adder, with carry-in and carry-out
- Starting from the Truth Table derivation of the functions for Sum and Carry
- Implementation through logic gates and test on the board

Lab 3: A Real SoC



- Creation of an entire SoC with external peripherals
- Exploit the On-Board user interfaces for LEDs dimming
- Instantiation of a Processing System, external timers (PWM), and GPIO
- Implementation on the board, understanding of the need for a program to run and test

Lab 04: MNIST NN



- Hardware implementation of a simple MNIST neural network
- SoC utilization with custom peripherals
- Students can interact with Computers and Tablets
- Comparison between hardware-accelerated and software-elaborated neural network

Awards - Chen

Status update about the webinars

- 3-minute pitch video about CEDA and what it offers
  - using the EDA slides – presented by Miguel ? – play video at conferences/events
- short “importance of EDA” testimonials
  - 3-minute videos of ~10 persons (senior and junior) about EDA and CEDA – using predefined set of questions – recorded off-line (live at conferences?) - post them regularly and run them at conferences
- longer in-depth interview webinars :
  - ~8 longer interviews about history and future of EDA……
  - 1 interview every month……. broadcasted live + recorded for later viewing

 1) set up small committee, finalize the concept and speaker list (target: Nov-Dec 2024)

2) plan the on-line webinars one by one in 2025

20th Anniversary -

CEDA Publications

- Report by VP Publications -

Jörg Henkel

Oct 27th 2024

Update CEDA Publications

- Embedded System Letters
  - ESL will be bi-monthly starting from Feb. 2025

- Design & Test Magazine
  - EiC Partha Pande has successfully led the magazine for first term (3 years)
  - Motion for second term (2 years)

Status of D&T

Partha Pande, EIC

Mehdi Tahoori, A-EIC

Oct. 2024

Accomplishments so far:

- Special issues on various topics
- New initiatives
- Revamping interview articles
- Faster turn around

Issues in 2024

- Jan/Feb: SI: Ethics in Computing (4 plus editorial), 4 general interest, 1 tutorial, 2 Reports, Last Byte, From the EiC
- Mar/Apr: SI: 2021 Workshop on Top Picks (6 plus editorial), 3 general interest, 2 Reports, Last Byte, From the EiC
- May/Jun: 7 general interest, 2 Reports, Last Byte, From the EiC
- Jul/Aug: SI: Silicon Lifecycle Management (6 plus editorial), Interview, Last Byte, From the EiC
- Sept/Oct: SI: Post-Quantum Cryptography for Internet-of-Things (4 plus editorial), general interest papers (3), From the EiC
- Nov/Dec: SI: Open-Source Silicon (3 plus editorial), Tutorial, 4 general interest, 1 Roundtable, Report, 2 Obituaries, Last Byte, From the EiC

New Special Issues

- Wearable IoT Devices
- Top Picks of Security 2022
- tinyML
- SBCCI 2023
- 2024 Top Picks
- 3D NAND Flash Storage

New Initiatives

- Top Pick on Reliability and Test
  - First edition was completed and selected
    - First round selected (12 out of 30+ submissions) and presented at Top Picks Workshop collocated with ITC 23
    - The top picks selected (6) and now invited for publication in SI
  - 2nd edition is going on
- New SIs related to Test
  - Silent Data Corruption (SDC): In planning
    - GEs: Dimitris Gizopoulos (U Athens), Sriram Sankar (Meta), Mehdi Tahoori (KIT), Yervant Zorian (Synopsys)
  - D2D UCIe design and test
    - In planning: GE: Debendra Das Sharma, Yervant Zorian
- Journal first model with NoC Symposium

Interviews

- We have revamped this
- Some examples
  - Janet Olsen
  - Sung-Mo "Steve" Kang
  - Vishwani Agrawal
  - Janusz Rajski
  - Yao-Wen Chang (with transcriber)

Turn around time

- Information based on manuscripts with an original submission date of on or before 31st December 2021:
  - Days to first decision (all manuscripts): 83.38
  - Days to first decision (with final decision only): 81.74

- Information based on manuscripts with an original submission date of on or after 1st January 2022
  - Days to first decision (all manuscripts): 45.08
  - Days to first decision (with final decision only): 40.04

Road Ahead

IEEE Design and Test (Video) Roundtables

- A series of quarterly events as D&T zoom-based video roundtables making it lively.
- We need to increase the number of roundtables
- Plan for 3-4 roundtables per year (is this too many?)
- Maybe open it to the public or keep it closed? (try both options?).
- Share IEEE D&T roundtable videos via IEEE D&T website. (create a place for IEEE D&T roundtable videos; could be one of the free IEEE D&T resources?).
- Each D&T roundtable may include 3 visionaries + moderator. 1-2 visionaries from industry; 1-2 from academia; last for 60 minutes. Q&A type format Sample topics:
  - Test vs Trust (Rob Aitken, Serge Leef, M. Tehranipoor and S. Mitra; Moderator Ramesh (Done)
  - ML for EDA; Moderator Y. Chen or Hai Li.
  - Resurgence of High-Level Design Paradigms: Moderator Luca Carloni; HLS leads from Cadence, Synopsys and Mentor, Jason Cong UCLA

Perspectives

- Covers general interest topics, 4-8 pages, with very few references.
- Retrospective and forward-looking
- It is usually from senior people in academia and industry
- Since they are reviewed can they be considered for impact factor?
- Potential topics and authors
  - Reliability
    - Jacob Abraham
    - Ravi Iyer
    - ?
  - Testing
    - **Janusz Rajski Done**
    - John Hayes
    - Hans-Joachim Wunderlich
    - ?
  - EDA
    - **Giovanni DeMicheli DONE**
    - Masoud Pedram
    - Alberto Sangiovanni-Vincentelli
    - ?

General Interest Papers

- Explore means to increase the number and quality of general interest papers.
- Use of social media to address this.
- Advertise the faster turn around time to the community in conferences.

Initiatives

Qi Zhu

October 27, 2024

Initiatives – CEDA Sponsored IEEE TCs

- Internet of Things (IoT)
  - https://iot.ieee.org/
  - CEDA representative: Theocharis Theocharides
- Smart Cities
  - https://smartcities.ieee.org/
  - CEDA representative: Maria Michael
- International Roadmap for Devices and Systems (IRDS)
  - https://irds.ieee.org/
  - CEDA representative: Ian O'Connor
- Taskforce on Rebooting Computing (TFRC)
  - https://rebootingcomputing.ieee.org/
  - CEDA representative: Qi Zhu

Initiatives – IEEE TCs

- CEDA representatives will attend corresponding TC's regular meetings, provide feedback, ideally involve in the decision-making process, and report back to the CEDA EC every 6 months.
- Positive interaction with IoT TC
- Smart Cities
  - Requesting a person from CEDA communication/outreach committee as a correspondent to their communication committee (providing access to Smart Cities social media channels for forwarding relevant information from CEDA)
  - Requesting two CEDA volunteers to work with them on technical tracks on cutting-edge cross-OU subjects
  - Other options on creating new common conferences/workshops

Initiatives – Budget

- Underspending in 2024
  - DATE YPP ($10K)
  - Student Travel Grant ($30K)
  - High-School Summer Camp with Member Societies ($30K)
  - EDA Special Sessions ($40K)
  - Special Session for CEDA Outreach Conferences ($32K)
  - Open-Source Implementation of Hardware Security Attacks and Countermeasures ($15K)
  - Tiny and Fair ML Design Contest ($10K)
- 2025 Initiatives
  - DATE YPP
  - Student Travel Grant?

IEEE CEDA Standards EC Update - ICCAD 2024

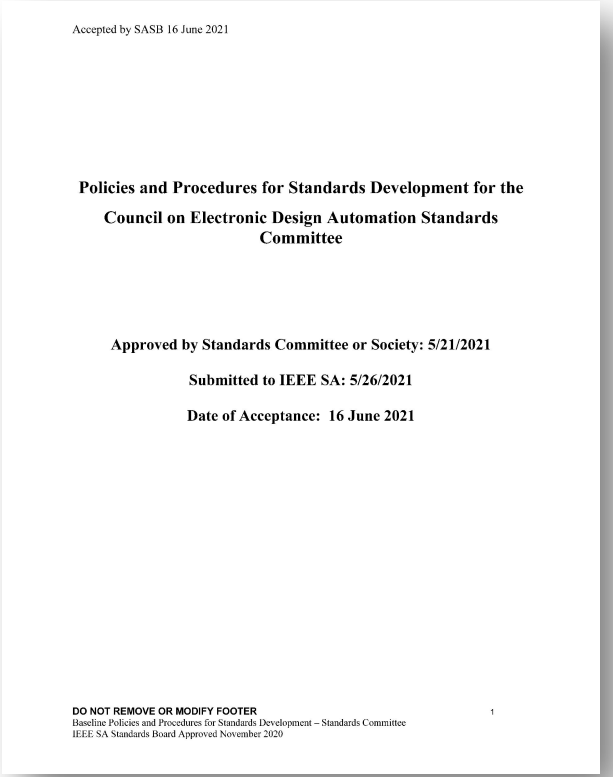
Aparna Dey
Vice-President of Standards, IEEE CEDA
Chair –CEDA Standards Committee
October 27, 2024

Standards Committee Mission /Objectives

- Drive Standardization in advanced EDA topics with focus on "research-based topics"
  - Proposals from Academia, and Industry Adv. Research groups
  - Collaborate/ Joint sponsor w/ IEEE DASC & other Industry Standards organizations/committees
  - Leverage CEDA Events/Network/CEDA Standards site to promote SC standards activities, invite new members and proposals, panel discussions, presentations, SC f2f meetings,

Current Status & Achievements

- CEDA SC Leadership - meeting Quarterly
  - Next F2F Officers meeting at Cadence, San Jose -12/13/2024
  - Aparna Dey, chair (CEDA- VP Standards), Dennis Brophy (Vice-chair) Yatin Trivedi (Secretary)
- CEDA Standards Committee update
  - Increased membership through new CEDA Standards site – 20+ new members (Top EDA companies, Univ, User companies)
  - Working on a new proposal for HI/Chiplets Benchmarking Standard with IEEE Packaging group
  - AI /ML infrastructure in EDA



Accepted by SASB 16 June 2021

Policies and Procedures for Standards Development for the Council on Electronic Design Automation Standards Committee

Approved by Standards Committee or Society: 5/21/2021

Submitted to IEEE SA: 5/26/2021

Date of Acceptance: 16 June 2021

DO NOT REMOVE OR MODIFY FOOTER
Baseline Policies and Procedures for Standards Development – Standards Committee
IEEE SA Standards Board Approved November 2020
1

Potential Areas for Standardization

- AI/ML in EDA
- 3D/2.5D, Chiplets design, Standard Format
- Photonics
- Digital Twin
- Functional Safety
- Low Power
- Thermal Constraints
- Functional Verification
- Simulation

Current Activities Update

- Meeting with IEEE TC-EDMS committee to explore possible collaboration in HI and Chiplets area -9/17
- Presented IEEE CEDA Standards update to IEC TC 91 WG 13 (EDA) annual meeting -9/24
- Meeting regarding ML in EDA with Open EDA group
- Applied for TCOS funding for full-day CEDA Standards workshops
- IEEE AI Coalition meeting – Attended regular meetings and F2F on 11/7
  - Participating in AI Hardware Subcommittee WG meeting 8/24, 10/24
    - Identifying gaps for possible standardization efforts

Heterogenous Integration and Chiplets update – IEEE TC-EDMS (Electronic Design, Modeling & Simulation)

- CEDA SC Officers invited CEDA standards to present to the IEEE TC –EDMS Benchmarking committee – 9/17
- Pavel P. /Heidi B./Vladimir O. presented TC –EDMS Benchmark efforts with respect to Electronic Packaging
- Next step- To discuss possible standardization scope in HI and Chiplets and propose a CEDA Standards WG.

IEEE AI Coalition

Representatives from across IEEE who have come together with a shared purpose:

To catalog all of IEEE's AI-related resources and activities into a cohesive platform, and foster a robust, cross-disciplinary network of IEEE expertise in AI.

Artificial Intelligence Coalition meeting 6 June 2024

- Held at the Microsoft New England Research and Development Center (NERD), Cambridge, MA
- 37 attendees and 28 in person
- Analysis conducted for AI content across IEEE
  - Looked for gaps in coverage
  - Will form activities around those gaps
- AI Policy presented by IEEE USA and European Office
- Heard from volunteers and staff how IEEE is using AI as an organization
- Discussed long term vision of the AI Coalition
- Attended Imagination In Action at MIT on 7 June
- Heard from our first project “TinyML”

- Next Steps: Top gaps identified
  - AI Technology - Advancing Hardware topics in AI
    - Action: Work with Leadership Team to identify experts to lead this effort (Computer Society, CIS, etc)
    - Meeting in August, October 2024
  - Social Implications, partner with Tech Ethics and SSIT
    - Social implications related to implementation
    - Responsible AI
    - Technology to Verify AI Models and Data to build Trust and Understanding
    - Action: Recruit leadership / form subcommittee
  - Future Tech Forum / AI Coalition Event
    - Nov 7, 8 2024 NERD Center Cambridge, MA
    - Will invite Imagination in Action to collaborate

IEEE AI Hardware Sub-committee – August 2024

These are the technical topics mentioned in our first meeting

- AI chip energy efficiency
- AI chip security
- Standards for AI chip design (Is this mainly interfaces? Compute cores will vary)
  - A list of AI hardware standards priorities/needs might be worthwhile?
- AI chip design aligned with ethical guidelines to minimize harm/misuse
- R&D for AI hardware to keep pace with rapidly evolving demand
- Sustainable practices for manufacturing and disposal of AI hardware/chips
- Performance: Drive more powerful, efficient, secure, and accessible AI hardware
  - Significant overlap w the other items
- Test benches (Performance benchmarks - is there a testing procedure for these specific kinds of chips?)
- Power management and power consumption control (load balancing/shifting)

IEEE AI Coalition Mission

Key objectives:

1. **Classify and Index AI Work**
   - Organize and categorize AI-related work from across IEEE
   - Create a user-friendly gateway for anyone to easily discover and engage with it
   - Reinforce IEEE as an authority on AI with touchpoints to the Societies, Councils and other major groups working in the IEEE AI ecosystem
2. **Enhance IEEE Services with AI**
   - Understand how artificial intelligence is already used to enhance the services provided by IEEE
   - Explore new ways to leverage AI for optimizing processes, improving the member experience, or advancing technical publications

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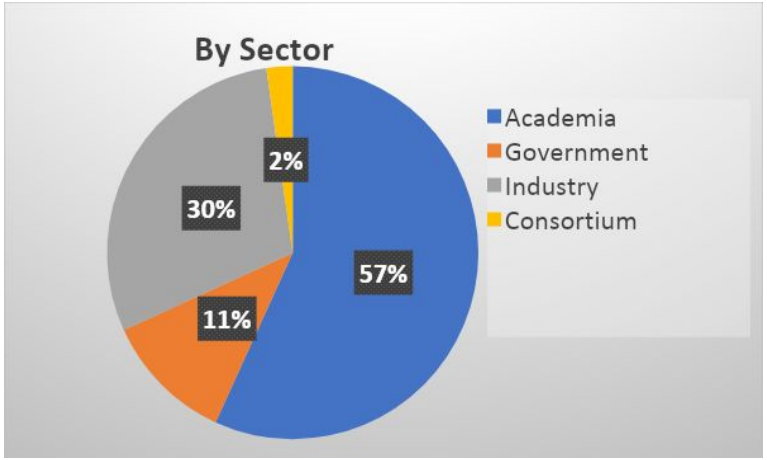
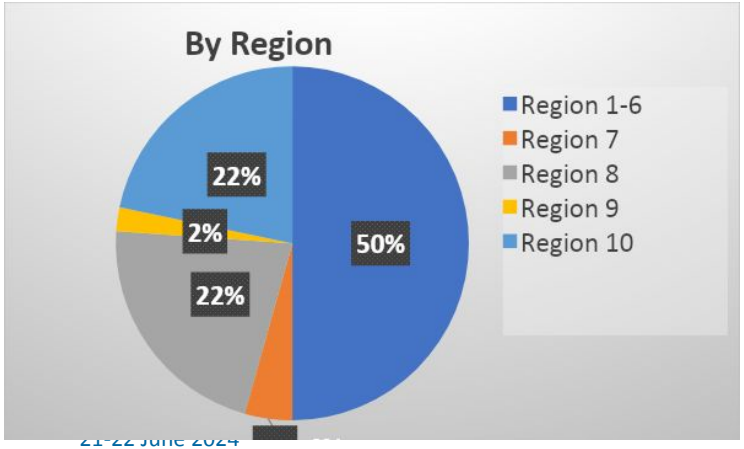
3. **Find and Fill Gaps**
   - Use our comprehensive view of AI-related projects and content within IEEE to identify gaps in coverage
   - Launch new projects and activities to fill those gaps

IEEE AI Coalition

Diverse Makeup:

- **44 representatives**
  - 33 IEEE Societies and Councils
  - Other IEEE groups and special appointments (Standards Assn., TechEthics, Entrepreneurship, and more)
  - IEEE Staff from TA, IT, Legal, IEEE-USA, IEEE Europe
- **Demographics by Sector**
  - Academia - 25
  - Industry - 13
  - Government - 5
  - Consortium - 1
- **Demographics by Region**
  - Region 1-6 - 23
  - Region 8 - 10
  - Region 10 - 10
  - Region 7 - 2
  - Region 9 - 1





Questions?

Young Professionals Coordinator

Iris Hui-Ru Jiang

October 27, 2024

YP Activities – DAC

- Co-sponsor the YP events with SIGDA

DAC Young Fellow Program is not included

Event		Lead
Early Career Workshop Organizers: Zhiding Liang (RPI), Rickard Ewetz (UCF), Mengxin Zheng (UCF), Ganapati Bhat (WSU) Speakers from LBNL, NYU, PNNL, JHU, NSF, Gatech, JHU, UW-Madison, UPenn, Northeastern University, Duke, UT Austin, UT Dallas, Argonne, Synopsys, JPMC, Microsoft.		SIGDA
PhD Forum Organizers: Yingyan (Celine) Lin (Gatech), Vidya Chhabria (ASU), Guohao Dai (Shanghai Jiao Tong Univ.)	colocated	CEDA
University Demo Organizers: Umamaheswara Rao Tida (North Dakota State Univ.), Nan Wu (George Washington Univ.), Sumitha George (North Dakota State Univ.)		CEDA
System Design Contest Organizers: Meng Li (Peking Univ.), Qi Sun (Zhejiang Univ.), Sitao Huang (UC Irvine), Atefeh Sohrabizadeh (UCLA)		SIGDA

Ph.D. Forum at DAC

The Ph.D. Forum at the Design Automation Conference is a poster session hosted by ACM SIGDA and IEEE CEDA for Ph.D. students to present and discuss their dissertation research with people in the EDA community. It has become one of the premier forums for Ph.D. students in design automation to get feedback on their research and for industry to see academic work in progress: hundreds of people attended the last forums. Participation in the forum is competitive with acceptance rate of around 30%. Limited funds will be available for travel assistance, based on financial needs. The forum is open to all members of the design automation community and is free-of-charge. It is co-located with DAC to attract the large DAC audience, but DAC registration is not required in order to attend this event.

34th ACM SIGDA/IEEE CEDA University Demonstration

Date: June 24, 2024

Location: Moscone Center West, San Francisco

DAC System Design Contest

Overview:

The DAC System Design Contest focuses on object detection and classification on an embedded GPU or FPGA system. Contestants will receive a training dataset provided by Baidu, and a hidden dataset will be used to evaluate the performance of the designs in terms of accuracy and speed. Contestants will compete to create the best performing design on a Nvidia Jetson Nano GPU or Xilinx Kria KV260 FPGA board. Grand cash awards will be given to the top three teams. The award ceremony will be held at the 2024 IEEE/ACM Design Automation Conference.

CEDA
IEEE Council on Electronic Design Automation

YP Activities – ICCAD / SMACD

- ICCAD
  - Co-sponsored YP events with SIGDA: SRC / CADathlon / Job Fair / TinyML
  - CEDA sponsored event: CAD Contest
- SMACD
  - EDA Competition approved in Feb. EC meeting

Student Travel Grants Plan: 2024/10/15 Update

- ESWEEK: 6K (5K in 2023)
- ICCAD: 6K (5K in 2023) for student presenters

  5K (4.8K in 2023) for CAD contest winners

  4~5K for CADathlon, Design Contest, and Job Fair
- DAC / DATE / ASP-DAC: merge with YP events
- MLCAD 2024: 3K
- AsianHOST 2024: 3K
- Other workshops and ad-hoc applications: planning up to 2~3K
  - https://ieee-ceda.org/ieee-ceda-student-travel-grant-program

Publicity - Parameswaran

Conferences

Tsung-Yi HO

October 27, 2024

Sponsored conferences/events (2024.1 ~)

- Financial Sponsorship (20)

MLCAD (50%)	ICCAD (46.67%)	ETS (25%)
DTTIS (25%)	VLSI-SoC (25%)	MPSoC (33%)
LAD (100%)	LATS (25%)	MEMOCODE (25%)
ISLPED (15%)	SIES (50%)	ITC-Asia (50%)
DAC (50%)	ASP-DAC (12.5%)	DDECS (25%)
CODAI (25%)	SBCCI (5%-7%)	ATS (25%-50%)
IOLTS (100%)	DATE (29.03%)	

- Technical Sponsorship (12)

FMCAD	LASCAS
GLSVLSI	ICITES
ISPD	ISED
SMACD	AsianHOST
FDL	ISEDA
VLSID	COINS

CEDA Flagship Conferences in 2025

- ASP-DAC (January 20-23@Tokyo)
  - Kazutoshi Wakabayashi
- DATE (March 31-April 2@Lyon)
  - Cristiana Bolchini
  - David Atienza
- DAC (June 22-25@San Francisco)
  - Gi-Joon Nam
  - Luis Miguel Silveira
- ESWeek (September 28-October 3@Taipei)
  - Christian Pilato
- ICCAD (October 26-31 or November 2-7@Munich)
  - Jiang Hu

Unfinished Business -

- Technical Activities

CEDA Technical Activities

Ian O'Connor, Vasilis Pavlidis

October 27th, 2024

Agenda

- CEDA Chapters: News, Chapter award
- MTO CEDA Technical Committees
- One-off event sponsorship
- Distinguished lecturer program – now handled by Vasilis
  - Class 2023-2024 + 2024-2025
  - Virtual Distinguished Lecturer program
- Luncheon Keynote speakers

CEDA Chapters

13 active Chapters

2023
Bangalore
Beijing
Central Illinois
Chengdu
Guangzhou
Hong Kong
Japan
Pennsylvania
Russia
Shanghai
South Brazil
Spain
Switzerland
Taipei
Tunisia
Kenya

2024
Bangalore
Beijing
Central Illinois
Chengdu
Central Penn.
Guangzhou
Hong Kong
Kenya
Shanghai
South Brazil
Spain
Switzerland
Taipei

Dormant Chapters (no 2024 funding)

Central Texas
Japan
Montreal
Morocco
Russia
Seoul
Tunisia

Potential new Chapters?

Boston
San Francisco Bay area
France – 2025 ?
Belgium – 2025 ?
Germany
Italy
Portugal
Turkiye

Report on chapter update meeting @ DAC 2024

- Monday June 24th 5pm-7pm PDT
- Attendees:
  - Aloke Kumar Das (Bangalore Chapter) (remote)
  - Yangdi Lyu (Guangzhou Chapter) (remote)
  - Skanda Raghavendra (Bang. student branch)
  - Yutaka Tamiya (Japan joint Chapter) (remote) – unfunded in 2024, to rectify for 2025
  - Baris Taskin (Pennsylvania Chapter) (remote)
  - Wenjian Yu (Beijing Chapter) (remote)
  - Zhiyao on behalf of Ray Cheung (Hong Kong Chapter) (remote)
  - Ing-Chao Lin (Taipei Chapter)
- Very good activity reported across the board
- Some issues accessing CEDA Currents (now resolved)

Report 2024 activities and spending
Plan 2025 activities and budget
Flag any issues

CEDA Chapters – gearing up for annual reports

- Financial Sponsor
  - Supported 12 proposals in 2024
  - Total funding for all chapters around 40k$
- Chapter Report
  - vTools
- Budget Allocation
  - Group event: seminars, meetings, summer course, DL, etc.
  - Special event: contest, awards, etc.
  - General expense: banner, local travel, souvenir, etc.
- Role Rotation
  - Chair, Vice Chair, Treasurer/Secretary
  - Term of service
- Virtual meeting to be set up for December

Chapter formation

- Member & Geographic Area resources:
  - Formation : https://mga.ieee.org/volunteer-hub/geographic-unit-operations/formations-and-petitions#changechapter
  - Application (with IEEE member acct): https://live.runmyprocess.com/live/2215365968/appli/233967?P_mode=LIVE&P_version=
- Possible new France Chapter (under discussion)

Petition to form an IEEE Society/Technical Council Chapter and Joint Chapter

A Chapter shall be a technical subunit of a Region, one or more Sections, or a Geographic Council. There may be single Society Chapters, joint Society Chapters, and Technical Council Chapters. Chapters are your local link to the valuable resources available from IEEE and its 40+ Societies and Technical Councils.

ORGANIZERS	• The Organizer (and Co-Organizer, if applicable) must be an active IEEE member of Graduate Student Member grade or higher for a minimum of 6 months • The Organizer (and Co-Organizer, if applicable) must be an active member of the Society(ies) or Council(s) involved • The Organizer shall serve as the interim Chapter Chair pending election at a later date *Note: For Joint Section Chapters, there must be one Organizer/Co-Organizer from each contiguous section involved.*
ENDORSERS	Chapter petitions must be endorsed by the following: • Section Chair Joint Sections Chapter petitions must be endorsed by the following: • Section Chair for each Section involved *Note: If the Organizer does not report to a Section, the petition will be endorsed by the Region Director.* Endorsers will be invited to endorse the petition once the petition has been verified by IEEE Staff.
PETITIONERS	Chapter petitions must be signed by the following: • 12 active IEEE members of Graduate Student Member grade or higher for a minimum of 6 months, who are members of the parent Society(ies) and Section(s) involved Qualified members will be invited to sign the petition once the petition has been endorsed by all Endorsers.
APPROVERS	Chapter Petitions must be approved by the following: • Region Director (or their designee) • Society/Council President, for each Society/Council involved Approvers will be invited to approve the petition once the petition has been signed by 12 Petitioners.

Chapter of the Year Award

- **Description:** To recognize the CEDA Chapters with the best yearly activities in the categories of chapter-sponsored technical activities. Award will recognize their contribution with consideration of quantity and quality of the activities implemented by the chapters.
- **Prize:** $1000 and Certificate to the Chapter of the Year. Presented to the chapter chair and must be used to fund chapter activities.
- **Funding:** Funded by the IEEE CEDA. Award is funded via CEDA Award Fund in the IEEE Foundation.
- **Presentation:** Annually at ICCAD
- **Basis for Judging:** The awards criteria include number and quality of chapter activities, percentage of attending sponsored events, membership development activities and chapter growth, local conferences/symposia/workshops, participation in the Distinguished Lecturer Program, involvement of students and YP members, contributions to newsletter, and timeliness of reporting of prior year.
- **Eligibility:** The winning chapters must be IEEE CEDA chapters. Self-nominations are allowed.
- **Nomination Details:** Previous winners of are not eligible for the same award within 3 years from the receiving the last award.

One-off event sponsorship

- SWEAT 2024, Bangalore, June 28th 2024 (1000USD) - Symposium-cum Workshop on Emerging AI/ML Trends www.sweat.ieee bangalore.org (organized by newly-formed CEDA Bangalore section) -> Prominent visibility for CEDA material, funding event lunch, remote CEDA address (Ian)
- DSD 2024, Paris, August 28-30 2024 (1000USD) - 7th Euromicro Conference Series on Digital System Design (potential future CEDA France Chapter) -> CEDA exposure through various channels (signage, printed materials, website listings, social media mentions, and email marketing campaigns)

Distinguished Lecturer Program

Class of 2023-2024

Available as of 1 August 2023

Vivek De

Distinguished Lecturer

2023 - 2024

More details →

Rolf Drechsler

Distinguished Lecturer

2023 - 2024

More details →

Prabhat Mishra

Distinguished Lecturer

2023 - 2024

More details →

Qinru Qiu

Distinguished Lecturer

2023 - 2024

More details →

Cheng Zhuo

Distinguished Lecturer

2023 - 2024

More details →

Class of 2024-2025

Available as of 1 August 2024

Prof. Ricardo Reis

UFRGS, Brazil

Semi esign
Automatio Networks /
Trends on ation Tools
Tutorials : allenges in
IoT and on EDA
(extended sign, from

Prof. Sudeep Pasricha

Colorado State University, USA

Seminars: Artifici e Speed of Light /
Robust and S onnected and
Autonomous Veh ty Challenges with
Computing: fro gs to Datacenters
Tutorials : Optic AI Acceleration /
Machine Learning Navigation / Green
and Sus mputing

Ass. Prof. Bei Yu

CUHK, Hong Kong

Semina g in EDA:
Whe ale VLSI
Mask Language
Mode Enabling
Larg in EDA

Prof. Alberto Bosio

ECL, France

Seminars : AI H r Safety-Critical
Applications / T of the Hardware
Tutorials : Appl Neural Network
Systems / Early sis for Cross-layer
Soft Errors R ssor Systems

CEDA

IEEE Council on Electronic Design Automation

CEDA VDL Program

- 5DLs class of 2023-2024 + 4 DLs class of 2024-2025
- roughly monthly VDL webinars (Thursdays at 9:00 AM ET) hosted by TY

ICCAD 2024 CEDA Luncheon Keynote

- Scheduled for Tuesday October 29th 2024 12:00pm-1:30pm
- Prof. Sachin Sapatnekar
  - Distinguished Professor and Robert and Marjorie Henle Chair, Dept ECE, U Minnesota
  - https://www.ece.umn.edu/users/sachin/
  - automated layout generation for analog circuits, design of ML HW, ML algorithms for EDA
- complementarity to ICCAD keynotes already scheduled (Leon Stok, IBM / Philip Wong, Stanford / Dilma Da Silva, US NSF)

2025 CEDA Luncheon Keynotes

- Decision at last EC meeting to use 2025 flagship conference LK slots for 20th anniversary celebratory events / panels
- Holds for ASP-DAC 2025 and for DATE 2025
- Assume also true for DAC 2025, ICCAD 2025 ?

Administrative - Paul

- **No EC meeting in November (conflicts with TAB meeting series)**
- **Next EC meeting will be Friday, 6 December at 9:00 AM ET (virtually)**

- **Kuh Award**
  - **Revisions accepted by TABARC Chair**
  - **TABARC will review and vote in November**
  - **Proposal planned for TAB vote in February 2025**

- **2025 Chapter of the Year Award**
  - **Nominations open: 1 December 2024**
  - **Nominations due: 28 February 2025**
  - **Will this be awarded at DAC 2025?**

- **DINNER - Valenca Restaurant - 7:00 PM**
  - **Meet in the lobby at 6:40 PM for group rides**