IEEE Design&Test

Call for Papers for a Special Issue on

LLM-aided Hardware Design, Verification and Test

Aim and Scope

Large Language Models (LLMs) are advanced AI systems built on deep learning frameworks, particularly leveraging transformer architectures, that excel in processing and generating human languages. In the fields of software and hardware design, LLMs are proving to be transformative. Recently, several industrial organizations have employed LLMs to analyze and generate design code and optimize the layout and configuration of chips. The use of LLMs in chip design represents a significant advancement in the semiconductor industry, showcasing how AI can be harnessed to tackle the increasing complexity of modern hardware design. Recent studies have explored the automation of Hardware Description Language (HDL) generation using AI tools, particularly LLMs. In addition, LLMs are also emerging as powerful tools in the realm of hardware verification and testing. Their ability to process and understand vast amounts of textual data makes them well-suited for tasks like generating test cases, analyzing design specifications, and even identifying potential vulnerabilities. By leveraging LLMs, engineers can automate routine verification tasks, reducing the time and effort required while improving the overall quality of hardware designs. This special issue aims to introduce the design and test community to this emerging topic of LLM-based hardware design, verification and test. It aims to raise awareness of applications of LLM in various aspects of hardware design and their widespread use. The scope of this special issue spans the entire Electronic Design Automation (EDA) stack from design, verification, test, security to silicon lifecycle management. Through this special issue, we hope to build a cross-disciplinary community of researchers who are motivated by advanced LLM-aware hardware design paradigms.

Topics of Interest

This special issue is dedicated to LLM-based hardware design, verification and test. Topics of interest include (but not limited to):

- LLM-based digital circuit design
- LLM-based analog/mixed-signal/RF circuit design
- LLM-based design verification
- LLM-based assertion generation
- LLM-based synthesis
- LLM-based layout optimization
- LLM-based hardware security
- Applications of LLM for hardware testing
- LLM-based silicon lifecycle management

Submission Guidelines

Prospective authors should follow the submission guidelines for IEEE Design & Test. All manuscripts must be submitted electronically to IEEE Manuscript Central at https://mc.manuscriptcentral.com/dandt. Indicate that you are submitting your article to the *"LLM-aided Hardware Design, Verification and Test"*. Manuscripts must not exceed 5,000 words, including figures (with each average-size figure counting as 200 words) and a maximum of 12 references (30 for surveys). This amounts to about 4,000 words of text and a maximum of five small to medium figures. Accepted articles will be edited for clarity, structure, conciseness, grammar, passive to active voice, logical organization, readability, and adherence to style. Please see IEEE Design & Test Author Information at: https://ieee-ceda.org/publication/ieeedesign-test-dt/author-info.

Schedule

- Open for submissions: December 10, 2024
- Submission deadline: April 1, 2025
- First-round review decisions: June 15, 2025
- Deadline for revision submissions: June 30, 2025
- Notification of final decisions: August 15, 2025
- Tentative publication: Fall 2025

Guest Editors

Please direct any questions regarding this special issue to one of the following

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