



## DAYANANDA SAGAR COLLEGE OF ENGINEERING

Shavige Malleshwara Hills, Kumaraswamy Layout, Bangalore-560078

(An Autonomous Institute affiliated to VTU,

Approved by AICTE & ISO 9001: 2008 Certified)

Accredited by National Assessment & Accreditation Council (NAAC) with 'A' Grade

### Department of Electronics and Communication Engineering

### IEEE-CEDA DSCE CHAPTER

### Report

## Knowledge Insights on “NAND Flash Memory: Innovating To Meet World’s Storage Needs”

Date: 23<sup>rd</sup> November, 2024

The poster features a blue background with a gear and circuit patterns. It includes logos for Dayananda Sagar College of Engineering, CEDA, and IEEE. The text is centered and reads: 'DAYANANDA SAGAR COLLEGE OF ENGINEERING Department of Electronics and Communication Engineering IEEE - DSCE CEDA Chapter brings to you KNOWLEDGE INSIGHTS ON NAND Flash Memory: Innovating To Meet World's Storage Needs presented by Dr. Sudipta Dutta'. A photo of Dr. Sudipta Dutta is shown in a rounded square. Below the photo is her title: 'PRINCIPAL ENGINEER, WESTERN DIGITAL BENGALURU, KARNATAKA, INDIA'. At the bottom, there are two blue boxes: 'EVENT DETAILS' with date, venue, and time, and a list of faculty members and office-bearers.

**DAYANANDA SAGAR COLLEGE OF ENGINEERING**  
Department of Electronics and Communication Engineering  
IEEE - DSCE CEDA Chapter  
brings to you  
**KNOWLEDGE INSIGHTS**  
ON  
*NAND Flash Memory: Innovating To Meet World's Storage Needs*  
presented by  
**Dr. Sudipta Dutta**

**PRINCIPAL ENGINEER, WESTERN DIGITAL  
BENGALURU, KARNATAKA, INDIA**

**EVENT DETAILS**  
Date: November 23<sup>rd</sup>, 2024  
Venue: PC Sagar Auditorium  
Time: 9:30 am - 11:30 am

**CEDA-DSCE Faculty Advisor: Dr. P Vimala**  
**Faculty Co-ordinators: Dr. Thenmozhi | Prof. Chaitra A**  
**Office-Bearers: Indrani A | Sathvik Rao | Sumukh V | Dhaavani | Kavya P | Manohar M | Saadyant PR**

<b>Dr. B G Prasad</b> Principal, DSCE	<b>Dr. Suma V</b> Vice-Principal & IEEE SB Counselor, DSCE	<b>Dr. Shobha K R</b> Prof & HOD, ECE, DSCE Secretary, IEEE Bangalore Section	<b>Dr. Kiran Gupta</b> IEEE SB Advisor, DSCE
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A briefing of the session’s agenda was given by the CEDA-DSCE Student Secretary.

Dr. Sudipta Dutta was introduced and welcomed on stage by the CEDA-DSCE Student Webmaster.



The session focuses on how NAND flash memory technology has evolved to address the growing demand for efficient, reliable, and high-capacity digital storage solutions. From 2D to 3D NAND, advancements have significantly increased storage density, speed, and cost efficiency, enabling widespread use in SSDs and smartphones.



Innovations in cell architectures (SLC, MLC, TLC, QLC) balance capacity, performance, and reliability, while addressing challenges like wear-out and power consumption. As data-heavy applications like AI, IoT, and cloud computing expand, NAND continues to evolve with smarter controllers and sustainable practices, ensuring it remains a cornerstone of modern digital storage solutions.



Dr. Dutta also took questions from the audience and had an interactive exchange of words and gave insights on how to work better in industry-based projects. The session started at 10am and was concluded by 11:30 with a student crowd of 207.



A token of appreciation and gratitude was presented by IEEE CEDA-DSCE Student Chair. The session was concluded with a Vote of Thanks from the CEDA-DSCE Faculty, Dr. P Vimala.

