CALL FOR PAPERS

ASAP 2025

36th IEEE International Conference on Application-specific Systems, Architectures and Processors

July 28-30, 2025 (tentative)
Vancouver, BC, Canada

The 36th IEEE International Conference on Application-specific Systems, Architectures, and Processors (ASAP 2025) is organized by Simon Fraser University in Vancouver, BC, Canada, July 28 to 30, 2025. The history of the ASAP conference traces back to the International Workshop on Systolic Arrays, organized in 1986 in Oxford, UK. It later developed into the International Conference on Application-Specific Array Processors. With its current title, it was organized for the first time in Chicago, USA, in 1996. Since then, it has alternated between Europe and North America.

Important Dates

Abstract Submission Deadline
February 14, 2025

Paper Submission Deadline
February 21, 2025

Acceptance Notification
April 28, 2025

Camera Ready
May 20, 2025

Main Conference
July 28-30, 2025 (tentative)

The conference covers the theory and practice of application-specific systems, architectures, and processors, feature topics spanning the following areas:

- Accelerator Design, e.g., AI, big data, computational genomics, finance, network processing
- Application-Specific Instruction-Set Processors and Architectures
- Approximate and Autonomous Computing Systems
- Cloud Computing Accelerators
- Compression and Computer Arithmetic
- Cryptography and Security Architectures
- Design Methods, Tools, and Compilers for Application-Specific Systems
- Edge Computing and Cyber-Physical Systems, e.g., wireless, mobile, IoT
- Embedded Systems and Domain-Specific Solutions
- Heterogeneous Computing, e.g., embedded devices, HPC systems, data centers
- Reconfigurable and Custom Computing, e.g., FPGAs, CGRAs
- Signal and Image Processing Systems
- Simulation and Prototyping, e.g., validation, performance analysis
- System Quality Attributes, e.g., energy efficiency, fault tolerance, security
- Emerging Technologies in Systems, e.g., optical computing, 3D devices and interconnects, memristors for storage and logic, in-memory computing, quantum computing

Organizing Committee

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Guidelines for Submissions

- All papers must be unpublished original research.
- All papers will be reviewed by at least three members of the program committee, with a double-blind review process.
- Manuscripts for full papers should not exceed 8 single-spaced, double-column pages using 10-point size font on 8.5x11 inch pages (IEEE conference style), including references, figures, and tables.
- Manuscripts for short papers should not exceed 4 single-spaced, double-column pages.
- All papers must be submitted electronically in PDF format.
- All accepted papers must be presented by one of the authors in order to be included in the proceedings and published in the IEEE Xplore Digital Library.

Submission link here

Questions:
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