CALL FOR PAPERS

IEEE Journal on Exploratory Solid-State Computational Devices and Circuits

Special Topic on Challenges and Opportunities for Information Processing and Storage with Ferroelectric Devices and Circuits

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Aims and Scope

The continued scaling of CMOS has been one of the key drivers towards the progress of modern computing. Miniaturization of advanced logic and memory has allowed us to achieve higher performance, reduced power consumption, and increased storage capacity. As the industry approaches the physical limits of conventional silicon scaling, new materials and devices need to be explored to continue this trend. Furthermore, new forms of computing need to be explored for making breakthrough advancements in hardware accelerator designs that can support the ever-growing size and complexity of the AI models.

Ferroelectric materials, with their unique property of spontaneous polarization that can be reversed by an external electric field, are promising candidates that can augment or replace conventional silicon-based semiconductor devices and act as scaling boosters for memory technology and enable new forms of information processing. For example, ferroelectric materials naturally exhibit non-volatile memory characteristics making them ideal candidates for memory application. By integration ferroelectric materials in the gate stack of a conventional silicon transistor, as an integrated capacitor with an access transistor and as a replacement for conventional charge-trap layers, new memory technologies in the form of ferroelectric field-effect transistor (FeFET), ferroelectric random-access memory (FeRAM) and ferroelectric NAND flash (Fe-NAND) can be realized. These can in turn enable orders of magnitude improvement in the storage capacity, energy-efficiency and latency for cache, DRAM and flash memories. Beyond conventional memories, ferroelectric devices also exhibit unique properties including multilevel polarization states and temporal dynamics, making them suitable for mimicking biological neural networks. As such, building digital, analog or mixed-signal circuits with ferroelectric devices can offer potential breakthroughs in energy-efficient, brain-inspired computing, overcoming the bottleneck of traditional von Neumann computing.

Such promising opportunities also come with practical challenges pertaining to choice of materials, scalability, performance, reliability and integration with CMOS. For example, aggressive scaling of ferroelectric materials for compatibility with advanced CMOS nodes can degrade their inherent ferroelectric behavior. Ferroelectric materials and devices suffer from fatigue, imprint, and retention issues, which can affect their long-term performance and reliability. Achieving high-speed switching comparable to SRAM remains a significant challenge. Finally, conformal deposition of ferroelectric materials with uniform properties across high aspect ratio 3-D structures is challenging, particularly for highly integrated devices.

This special issue of the IEEE Journal on Exploratory Computational Devices and Circuits (JXCDC) aims to call for the recent research advances that address both the challenges and opportunities for information processing and storage with ferroelectric devices and circuits. Papers on co-design and optimization across multiple domains including materials, devices, circuits and architecture/systems are encouraged.

Topics of Interests

Prospective authors are invited to submit original works and/or extended works based on conference presentations on various aspects of information processing and storage with ferroelectric devices and circuits. Topics of special interest include but are not limited to:

- Advancements in ferroelectric materials and devices addressing key challenges.
- Across-the-stack co-design and optimization approaches from materials and device to application.
- Monolithic and/or heterogeneous 3D integration with CMOS.
- New digital, analog and mixed-signal circuit design including peripherals for energy-efficient information processing and high-density storage.
- Architectural-level design for energy-efficient information processing and high-density storage.
- Application-level advancements for energy-efficient information processing and high-density storage.

Important Dates
Open for Submission: Feb. 15, 2025
Submission Deadline: May 15, 2025
First Notification: June 15, 2025
Revision Submission: July 1, 2025
Final Decision: July 15, 2025
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Please refer to the JxCDC website for submission guidelines.