MPSoC'25

23rd edition of the MPSoC event

June 15th-20th, 2025,

Hotel "les Fermes de Marie", Megève, France

This year, the MPSoC forum feature an outstanding program with 60 world-class R&D speakers to cover the key topics for **decentralized** architectures targeting **AI and embedded computing**. The experts discuss fundamental and strategic issues to master advanced technologies for **SW vs. HW design** and **semiconductor manufacturing** to build **energy efficient** many-core and **many IP** architectures.

More information on program and registration will be available at:

http://www.mpsoc-forum.org/

Focus

Multicore and Multiprocessor SoCs (MPSoCs) started a new computing era, but brought a twofold challenge: building HW easy to use by SW designers and building SW that fully exploits HW capabilities. The main domains addressed at MPSoC Forum are related to adapting HW and SW for better cost, performances and energy efficiency of next generation computing systems. Emerging SW and HW design technologies and architectures combined with advanced semiconductor manufacturing technologies are explored to build energy efficient multicore architectures serving advanced computing (image, vision, IA and cloud) and distributed networked systems.

Why attend

Thanks to its full week format and the high quality of both attendees and speakers, MPSoC is a unique opportunity for executives and senior managers to explore new ideas and refine strategic thinking. MPSoC is the single best event in the world that brings together so many leading thinkers on the future of HW and SW design. It enables great informal networking and interactions with experienced, distinguished researchers and top academic and industrial experts. It builds bridges between different technical areas and corporations, institutes and countries. Finally, it is a unique environment for anyone who wants to share knowledge with researchers and key managers from industry.

Contents

MPSoC is an interdisciplinary forum bringing together key R&D actors from the different fields required to design Multicore and multiprocessor HW and decentralized SW systems. The program brings together experts in major HW and SW architectures (Processor, Memory, I/O, Interconnect, RTOS, GFX, Virtualization, application-(domain) specific acceleration & systems, Data and cloud architectures), design technologies (parallel programming, rapid prototyping, system design models and tools) and emerging semiconductor technologies (heterogeneous integration, 3D, photonics) to build next-generation thinking that will bridge the gap between HW and SW. Around 60 world class R&D speakers will discuss fundamental and strategic issues to master Software-defined Hardware for energy-efficient and high-performance computing.

The program includes keynotes on major HW and SW trends and technical sessions to present strategic directions and state-of-the-art research. The 5-day program will also include in-depth technology challenge presentations and short keynotes followed by insightful panels. All the talks will be given by CTO-level speakers from Industry and world class professors from Academia.

For further information, please contact General Chair: Giovanni De Micheli
giovanni.demicheli@epfl.ch