IEEE/ACM
2025 INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN
ICCAD
44th Edition

CALL FOR PAPERS

DEADLINES

April 14, 2025
Abstract Submission Deadline

April 21, 2025
Paper Submission Deadline

April 21, 2025
Proposal Submission Deadline for Workshops, Tutorials, Special Sessions, Panels

June 6, 2025
Notification for Workshops, Tutorials, Special Sessions, Panels

June 30, 2025
Notification for Regular Papers

August 14, 2025
Camera-Ready Paper Submission

August 14, 2025
Author Registration Deadline

Jointly sponsored by IEEE and ACM, IEEE ICCAD is the premier forum to explore new challenges, present leading-edge innovative solutions, and identify emerging technologies in the electronic design automation research areas. IEEE ICCAD covers the full range of CAD topics – from device and circuit level up through system level, as well as post-CMOS design. IEEE ICCAD has a long-standing tradition of producing cutting-edge, innovative technical program for attendees.

COVERED TOPICS

Original technical submissions on, but not limited to, the following topics are invited:

- System-Level CAD
- Synthesis, Verification, Physical Design, Analysis, Simulation, and Modeling
- CAD For Emerging Technologies, Paradigms

More details on the covered topics and the submission process are provided on the following pages.

CALL FOR PROPOSALS

In addition to presentations of technical submissions, IEEE ICCAD will also cover

- Workshops
- Tutorials
- Special Sessions
- Panels
- Keynotes

More details on how to submit a proposal are provided on the following pages.

ORGANIZING CHAIRS

General Chair
Robert Wille
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Tutorial & Special Session Chair
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Workshop Chair
Ron Duncan
ron.duncan@synopsys.com

More information is available at 2025.iccad.com.

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Original technical submissions on, but not limited to, the following topics are invited:

1) System-level CAD

1.1 System Design

- System-level specification, modeling, simulation, etc.
- System-level issues for 3D integration
- System-level design case studies and applications
- HW/SW co-design, co-simulation, co-optimization, and co-exploration; emulation and rapid prototyping
- Micro-architectural transformation
- Multi-/many-core processor and heterogeneous SoC
- Memory and storage architecture and system synthesis
- System communication architecture, Network-on-Chip design
- Modeling, simulation, high-level synthesis, power/performance analysis, programming of heterogeneous computing platforms
- Application driven system design for big data
- Analysis and optimization of data centers
- AI for System Design

1.2 Embedded, CPS, IoT Systems and Software

- HW/SW co-design for embedded systems
- Compute, memory, storage, interconnect for embedded systems
- Domain-specific accelerators
- Energy/power management and energy harvesting
- Real-time software and systems
- Middleware, virtual machines, and runtime support
- Dependable, safe, secure, trustworthy embedded systems
- Embedded software: compilation, optimization, testing
- CAD for IoT, edge, and fog computing
- Modeling, analysis, verification of CPS systems
- Green computing (smart grid, energy, solar panels, etc.)
- CAD for application domains including wearables, health care, autonomous systems, smart cities

1.3 AI Algorithms and Applications

- New AI algorithms and applications
- New AI-driven design methodology
- AI algorithms and applications for embedded, CPS, IoT systems
- AI algorithms and applications on edge or in the cloud
- AI surrogate modeling for devices and circuits
- AI-based control, e.g., control for autonomous driving, or control in the cloud
- Security and privacy for AI algorithms and applications

1.4 CAD for AI

- CAD for AI accelerator design
- HW/SW co-design for AI algorithms and accelerators
- Neural architecture search for AI algorithms
- CAD for edge AI or online learning
- CAD for AI systems design in the cloud
- CAD for AI hardware on emerging technologies

1.5 Hardware Systems and Architectures for Artificial Intelligence

- Hardware and architecture for AI, Neural Networks, etc.
- Architecture designs for Edge AI, TinyML, etc.
- System-level design for (deep) neural computing
- Neural network acceleration including GPU and ASICs

1.6 Reconfigurable Computing

- Novel reconfigurable architectures (FPGA, CGRA, etc.)
- Neural network acceleration on reconfigurable accelerators
- High-level synthesis on reconfigurable architectures
- Compilers for reconfigurable architectures
- Reconfigurable fabric security
- HW/SW prototyping and emulation on FPGAs
- Post-synthesis optimization for FPGAs
- FPGA-based prototyping for analog, mixed-signal, RF systems
- AI for Reconfigurable Computing

1.7 Algorithms and Computing for Security

- New physical attack vectors or methods
- Supply chain security and anti-counterfeiting
- Privacy-preserving computation
- Homomorphic encryption and computation
- AI for security
- Security and privacy for AI algorithms and applications

1.8 Architecture and Systems for Security

- Hardware Trojans, side-channel attacks, fault attacks and countermeasures
- Nano electronic security
- Hardware-based security (CAD for PUF's, RNG, AES etc.)
- Split Manufacturing for security
- Design and CAD for security
- Trusted execution environments
- Cloud Computing data security
- Sensor network security

1.9 Low Power and Approximate Computing

- Power and thermal estimation, analysis, optimization, and management techniques for hardware and software systems
- Energy- and thermal-aware application mapping and scheduling
- Energy- and thermal-aware architectures, algorithms
- Energy- and thermal-aware dark silicon system design
- Hardware techniques for approximate/stochastic computing
- AI for low power and approximate computing

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2) SYNTHESIS, VERIFICATION, PHYSICAL DESIGN, ANALYSIS, SIMULATION, AND MODELING

2.1 High-Level and Logic

- New high-level/logic synthesis techniques
- Technology-independent optimization and technology mapping
- Functional and logic ECO (engineering change order)
- Resource scheduling, allocation, and synthesis
- Interaction between high-level/logic synthesis and physical design
- Acceleration algorithms for high-level/logic synthesis
- AI for high-level/logic synthesis

2.2 Testing, Validation, Simulation, and Verification

- High-level/logic modeling, validation, simulation
- Formal, semi-formal, and assertion-based verification
- Equivalence and property checking
- Emulation and hardware simulation/acceleration
- Post-silicon validation and debug
- Digital fault modeling and simulation analysis and optimization
- Delay, current-based, low-power test
- ATPG, BIST, DFT, and compression
- Memory test and repair
- Core, board, system, and 3D IC test
- AI for testing, validation, simulation, and verification

2.3 Cell-Library Design, Partitioning, Floorplanning, Placement

- Cell library design and optimization
- Transistor and gate sizing
- High-level physical design and synthesis
- Estimation and hierarchy management
- 2D and 3D partitioning. floorplanning, and placement
- Post-placement optimization
- Buffer insertion and interconnect planning
- AI for physical design

2.4 Clock Network Synthesis, Routing, and Post-Layout Optimization and Verification

- 2D and 3D clock network synthesis
- 2D and 3D global and detailed routing
- Package-/Board-level routing and optimization
- Chip-package-board co-design
- Layout and routing issues for optical interconnects
- Post-layout/-silicon optimization
- AI for clock network synthesis, routing, and post-layout optimization and verification

2.5 Design for Manufacturability and Design for Synthesis and Optimization Reliability

- Process technology characterization, extraction, and modeling
- CAD for design/manufacturing interfaces
- CAD for reticle enhancement and lithography-related design
- Variability analysis and statistical design and optimization
- Yield estimation and design for yield
- Physical verification and design rule checking
- Analysis and optimization for device-level reliability issues
- Analysis optimization for interconnect reliability issues
- Reliability issues related to soft errors
- Design for resilience and robustness
- AI for smart manufacturing and process control

2.6 Timing, Power, and Signal Integrity

- Deterministic and statistical static timing analysis, optimization
- Power and leakage analysis and optimization
- Circuit and interconnect-level low power design issues
- Power/ground network analysis and synthesis
- Signal integrity analysis and optimization
- AI for timing, power, and signal integrity

2.7 CAD for Analog/Mixed-Signal/RF and Multi-Domain Modeling

- Analog, mixed-signal, and RF noise modeling, simulation, test
- Electromagnetic simulation and optimization
- Device, interconnect and circuit extraction and simulation
- Behavior modeling of devices and interconnect
- Package modeling and analysis
- AI for analog/mixed-signal/RF and multi-domain Modeling

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3) CAD FOR EMERGING TECHNOLOGIES, PARADIGMS

3.1 Bio-inspired and Neuromorphic Computing

- Hardware for neuromorphic computing
- Event or spike-based hardware systems
- CAD for microfluidics
- CAD for biological computing systems
- CAD for synthetic biology
- CAD for bio-electronic devices, bio-sensors, MEMS

3.2 New System and Computing Paradigms

- Non-von Neumann architectures
- Quantum computing
- DNA computing
- Swarm intelligence
- Green computing
- New systems and technologies for AI, such as optical or quantum neural networks, large-scale chiplet-based systems, etc.

3.3 Nanoscale and Post-CMOS Systems

- New device structures and process technologies
- New memory technologies (flash, PCM, STT-RAM, memristor)
- Nanotechnologies, nanowires, nanotubes, graphene, etc.
- CAD for mixed-domain (semiconductor, nanoelectronic, MEMS, and electro-optical) devices, circuits, and systems
- CAD for nanophotonics and optical devices/ communication
- CAD for field-coupled nanotechnologies

SUBMISSION DETAILS

Paper submissions must be made through the online submission system **at the IEEE ICCAD website**.

Regular papers will be reviewed as finished papers; preliminary submissions will be at a disadvantage. Research papers with open-source software are highly encouraged where the software will be made publicly available (via GitHub or similar) with the camera-ready version if the paper has been accepted. For protecting the authors' identities in the double-blind review process, please do not include direct link to the non-anonymized software but indicate the open-source contribution on a textural basis only. Authors wanting to share GitHub repositories may want to look into using anonymous.4open.science which is an open-source tool that helps you to quickly double-blind your repository.

Authors are asked to submit their work in two stages. In stage one (abstract submission), a title, abstract, and a list of all co-authors must be submitted via the ICCAD web submission site. In stage two (paper submission), the paper itself is submitted whereby the submitted abstract of stage one can still be modified. Authors are responsible for declaring COIs, ensuring that their paper submission meets all guidelines, and that the PDF is readable.

DEADLINE FOR ABSTRACT AND PAPER SUBMISSIONS

The abstract submission deadline is **April 14, 2025 at 23:59 AOE**. No abstract submissions will be possible after this deadline.

The paper submission deadline is **April 21, 2025 at 23:59 AOE**.

We always have several authors contact the IEEE ICCAD office asking for a deadline extension. Due to the limited review cycle, NO extensions will be granted for ANY reason.

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REGULAR PAPER SUBMISSIONS

- All papers must be in PDF format only, with savable text and embedded fonts in included graphics.
- Each paper must be no more than 8 pages (including the abstract, figures and tables), double-columned, 9pt or 10pt font. One page of references is allowed, which does not count towards this 8-page limitation.
- ICCAD follows a double-blind review policy. Your submission must not include information that serves to identify the authors of the manuscript, such as name(s) or affiliation(s) of the author(s), anywhere in the manuscript, abstract, or in the embedded PDF data. References and bibliographic citations to the authors' own published works or affiliations should be made in the third person.
- Submissions of workshop papers without archived proceedings (or where the authors chose not to have their paper appear in the archived proceedings) or pre-prints, e.g., published on arXiv are allowed. Note, however, that the authors are expected to follow all reasonable efforts to ensure that the submission is compliant with the double-blind review process.
- Submissions not adhering to these rules or determined to be previously published or simultaneously submitted to another conference, or journal, will be summarily rejected.

IMPORTANT

Final camera-ready versions must be identical to the submitted papers with the following exceptions: inclusion of author names/affiliation, correction of identified errors, addressing reviewer demanded changes. No other modifications of any kind are allowed including modification of title, change of the author list, reformatting, restyling, rephrasing, removing figures/results/text, etc. The TPC Chairs reserve the right to finally reject any manuscripts not adhering to these rules.

TEMPLATES

Paper templates are available at the ICCAD website and authors are recommended to format their papers based on the IEEE template.

NOTIFICATION OF ACCEPTANCE

Authors will be notified of acceptance on or before, June 30, 2025. Final paper guidelines will be sent at that time.

PROCEEDINGS

The deadline for final camera-ready papers is August 14, 2025. Accepted regular papers or invited papers are allowed six pages plus one page of references in the conference proceedings free of charge. Each additional page (except references) beyond six pages is subject to the page charge at $150.00 per page up to the eight-page plus one page of references. IEEE will hold the copyright for ICCAD 2025 proceedings. Authors of accepted papers must sign an IEEE copyright release form for their paper.

CONFERENCE REGISTRATION

At least one author per accepted regular paper or invited paper must be registered to the conference by August 14, 2025. Failure to register will result in your paper being removed from the conference proceedings. IEEE reserves the right to exclude a paper from distribution after the conference (e.g., removal from the official proceedings) if the paper is not presented at the conference.

WILLIAM J. MCCALLA IEEE ICCAD BEST PAPER AWARD

Two papers from this year's ICCAD conference will receive this prestigious award. The winners will be chosen from nominated papers after a thorough and competitive process by the area specific selection committees and announced at the conference opening session.

IEEE ICCAD TEN-YEAR RETROSPECTIVE MOST INFLUENTIAL PAPER AWARD

One paper from the 2015 and 2016 editions of ICCAD will be selected for the 10-year retrospective most influential paper award as evidenced by impact on the research community as reflected in citations, on the vendor community via its use in an industrial setting or on new research venues as initiated by the paper during the past decade. Nominations from the community are welcome and can be sent to Ismail S. K. Bustany, Technical Program Vice Chair at **ismail.bustany@amd.com**.

CALL FOR PROPOSALS

Call for Workshop, Tutorial, Special Session, and Panel Proposals are all due on April 21, 2025.

WORKSHOP PROPOSALS

ICCAD provides a vibrant and supportive environment for small to medium-sized affiliated workshops. Typical workshops are one-day events on the Thursday of ICCAD. All workshop proposals should be emailed to Ron Duncan, Workshop Chair, at **ron.duncan@synopsys.com**.

TUTORIAL PROPOSALS

All IEEE ICCAD tutorials are embedded in the main technical program and free to conference attendees, providing value to attendees and a good audience for presenters. Typical tutorials run 1.5-2 hours, although longer tutorials (consisting of two session blocks of 1.5-2 hours each) may be considered. Tutorial proposals should not exceed two pages, should describe the topic and intended audience, and must include a list of confirmed participants/speakers with biographical data. Proposals should focus on the state-of-the-art in a specific area of broad interest amongst IEEE ICCAD attendees. All tutorial proposals should be submitted through the IEEE ICCAD website and questions can be addressed to Tsung-Yi Ho, Tutorial and Special Sessions Chair, at **ho.tsungyi@gmail.com**. Please read the proposal guidelines at IEEE ICCAD website.

SPECIAL SESSION PROPOSALS

Special Sessions typically run 1.5-2 hours. Special session proposals should focus on in-depth treatment on a topic of timely interest to the IEEE ICCAD audience. Special session proposals should not exceed two pages, should describe the topic and intended audience, and must include a list of confirmed participants/speakers with biographical data. All special session proposals should be submitted through the IEEE ICCAD website and questions can be addressed to Tsung-Yi Ho, Tutorial and Special Sessions Chair, at **ho.tsungyi@gmail.com**. Please read the proposal guidelines at **IEEE ICCAD website**.

1. Each co-author may contribute only one special session paper.
2. Include a paper abstract, author list, and designated speaker for each presentation in your session
3. Titles and author lists are final and cannot be altered, unless per feedback from the ICCAD 2025 Special Sessions Technical Program Committee
4. Speaker assignments are fixed and cannot be modified, unless per feedback from the ICCAD 2025 Special Sessions Technical Program Committee
5. No additional special session papers can be submitted other than those mentioned in the initial special session proposal
6. Please add the key word "Invited" in front of the camera-ready version title of each paper
7. Follow the same copyright release procedure as the regularly submitted papers

PANEL PROPOSALS

Research Panels are designed to engage a broad audience with timely and compelling topics. These sessions are meant to foster dynamic discussions, offering diverse perspectives on critical issues. Each panel lasts 1.5-2 hours. Panel proposals should not exceed two pages, should describe the topic, controversy, and intended audience, and must include a list of confirmed panelists with biographical data. Proposals should delve into a significant, overarching issue or question, featuring experts with differing viewpoints. The chosen topic should resonate with a wide range of ICCAD attendees, ensuring relevance across multiple segments of the community. All panel proposals should be submitted through the ICCAD website and questions can be addressed to Tsung-Yi Ho, at **ho.tsungyi@gmail.com**.

IF YOU NEED ASSISTANCE, PLEASE CONTACT THE APPROPRIATE COMMITTEE MEMBERS

General Chair: Robert Wille, **robert.wille@tum.de**

Program Chair: Deming Chen, **dchen@illinois.edu**

Vice Program Chair: Ismail S. K. Bustany, **ismail.bustany@amd.com**

Tutorial & Special Session Chair: Tsung-Yi Ho, **ho.tsungyi@gmail.com**

Workshop Chair: Ron Duncan, **ron.duncan@synopsys.com**