July 2019 Currents

CEDA
IEEE Council on Electronic Design Automation

CEDA Continues to Support Diversity in EDA

The second edition of the Advancing Diversity in EDA (DivEDA) workshop was held on Monday, June 3, 2019. This event was co-sponsored by IEEE CEDA and ACM SIGDA this year, and was co-located with the Design Automation Conference (DAC) at the Las Vegas Convention Center.

The overarching goal of DivEDA is to help facilitate women and underrepresented minorities (URM) advance their careers in academia and industry, and consequently, to help increase diversity in the EDA community. The first DivEDA forum was held at the Design Automation and Test in Europe (DATE) conference in 2018 in Dresden, Germany.

At DivEDA this year, Professor Soha Hassoun from Tufts University shared her experiences, both successes and challenges, that shaped her journey from EDA to Bio Design Automation. In addition to Hassoun's keynote, the DivEDA event contained three panels, where fifteen women and URM professors and senior researchers from industry provided practical tips on negotiation, work-life balance, and job hunting. The event concluded with an interactive mentoring session, which connected senior and junior researchers to ignite longer term mentorships.

The event attracted 45 attendees from all over the world, including from the US, Canada, Switzerland, Italy, China, Indian, Taiwan, Singapore and Hong Kong. The next DivEDA event is tentatively scheduled to be held in conjunction with DATE 2020 in Grenoble, France and IEEE CEDA looks forward to see more of its participants embracing next year's event!

CEDA Supports the 1st Workshop on Machine Learning for CAD (MLCAD)

CEDA committed to underpin activities for exploration of new approaches that prepare the next generation of design technologies for integrated systems supports the 1st Workshop on Machine Learning for CAD (MLCAD) that will take place in Canmore (Banff Area), Alberta, Canada on September 3-4, 2019.

The workshop focuses on Machine Learning (ML) methods for all aspects of CAD and electronic system design. The successor of this workshop was held at the Design, Automation and Test in Europe (DATE) Conference in March 2019. The workshop is sponsored by both IEEE Council on Electronic Design Automation (CEDA) and ACM Special Interest Group on Design Automation (SIGDA). Advances in machine learning (ML) over the past half-dozen years have revolutionized the effectiveness of ML for a variety of applications. However, design processes present challenges that require parallel advances in ML and CAD as compared to traditional ML applications such as image classification. As such, the purpose of the workshop is to discuss, define and provide a roadmap for the special needs for ML for CAD where CAD is broadly defined as design time techniques as well as run-time techniques.

Topics of interest to this workshop include but are not limited to: ML approaches to logic design, ML for physical design, ML for analog design, ML methods to predict aging and reliability, Labeled and unlabeled data in ML for CAD, ML for power and thermal management, ML techniques for resource management in manycores, ML for Design Technology Co-Optimization (DTCO).

There are two ways to participate to the workshop either as a presenter or as an attendee where graduate students especially are encouraged to participate. For more information and deadlines, please visit this link.

ASP-DAC 2020 – Call for Contributions

The 25th edition of the Asia South Pacific – Design for Automation conference will be held on January 13-16, 2020 in Beijing, China. ASP-DAC 2020 is the annual international conference on VLSI design automation in Asia and South Pacific regions, one of the most active regions of design and fabrication of silicon chips in the world. The conference aims at providing the Asian and South Pacific CAD/DA and Design community with opportunities of presenting recent advances and with

forums for future directions in technologies related to Electronic Design Automation (EDA). The format of the meeting intends to cultivate and promote an instructive and productive interchange of ideas among EDA researchers/developers and system/circuit/device designers. All scientists, engineers, and students who are interested in theoretical and practical aspects of VLSI design and design automation are welcomed to ASP-DAC. The areas of interest include but are not limited to: System-Level Modeling and Design Methodology, Embedded Systems and Cyberphysical Systems, Embedded Systems Software, Memory Architecture and Near/In Memory Computing, Neural Network and Neuromorphic Computing, Analog, RF, Mixed Signal, and Photonics, Low Power Design and Approximate Computing, Logic/High-Level Synthesis and Optimization, Physical Design, Design for Manufacturability and Reliability, Timing and Signal/Power Integrity, Testing, Validation, Simulation, and Verification, Hardware and Embedded Security, and Emerging Technologies and Applications. The paper submission deadline is July 5, 2019. For detailed instructions for submission, please refer to the "Authors' Guide".

HOST Symposium – Call for Contributions

IEEE International Symposium on Hardware Oriented Security and Trust (HOST) – the premier event aims to facilitate the rapid growth of hardware-based security research and development and highlight new results in the area of hardware security – has opened the call for contributions. Starting this year, HOST has two submission windows (August 15th and November 15th) with no abstract deadlines and no extensions. The 13th annual edition of HOST will be held 4-8 May 2020 in San Jose, California, the capital of Silicon Valley. HOST 2020 invites original contributions in all areas of overlap between hardware and security. Relevant research topics include techniques, tools, design/test methods, architectures, circuits, and applications of secure hardware. Starting this year, HOST has two submission windows with no abstract deadlines and no extensions. Papers can be submitted through the conference website by either August 15, 2019 (Summer Deadline) or November 15, 2019 (Fall Deadline).

VLSI Design 2020 – Call for Contributions

The 33rd edition of International Conference on VLSI Design (VLSID) and the 19th edition of the International Conference on Embedded Design will be held on January 4-8, 2020 in Namma Bengaluru, India. The theme of the conference this year is *Connecting Intelligent Systems to New Age Transistors*.

Semiconductors have made real what our ancestors would consider magic. The convergence of technology with modern life has reached a state where dependence of human life on semiconductor technology is ubiquitous. Intelligent systems are revolutionizing a variety of industries to help improve energy efficiency, quality, and flexibility of systems. To achieve these superior experiences, massive amount of researches are ongoing in the field of algorithms, embedded HW/SW design, IP core design and SoCs. These are well backed up by government policies, standards, and industry forums.

Incredible demand on functionality in a chip in a given power/thermal envelope forcing transistor geometries go smaller, which is imposing newer challenges in VLSI design and associated EDA tools/flows/methodologies. In 33rd International Conference of VLSI Design and 19th International Conference on Embedded Design, we plan to bring together all the leaders from industries, academia, industry bodies, government, standard organizations to go over all technology enablers in an "outside-in approach to design VLSI" which includes intelligent systems design, new techniques in algorithms, HW/SW/Protocol standards, core VLSI design, EDA tools/flows/methodologies and core silicon technologies. The paper submission deadline is July 7, 2019. More information and submission guidelines can be found here.

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Visit ieee-ceda.org/publication/esl-publication/author-guidelines.

***IEEE Design & Test* is open for submissions.**
Visit ieee-ceda.org/publication/ieee-design-test-dt/paper-submission-instructions.

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