March 2019

CEDA Currents

IEEE Council on Electronic Design Automation

DATE 2019 – Call for Participation

The DATE conference will take place at Firenze Fiera in Florence, Italy, from 25 to 29 March 2019 and will be chaired by Professor Jürgen Teich, Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), DE. For the 22nd successive year, DATE has prepared an exciting technical programme.

The registration to the conference is only possible via the online registration platform. Please kindly note that everyone who wants to attend the conference, the exhibition, or single sessions must register. The online registration for DATE 2019 is possible until Wednesday, 13 March 2019. Afterwards, the registration to the conference is only possible on-site at the registration desk and will result in an additional on-site charge of EUR 50.00.

On behalf of the whole DATE Executive Committee, we thank you very much in advance for your participation and are looking forward to welcoming you to DATE 2019 in Florence! More information and the programme can be found here.

Call for CEDA Distinguished Lecturers

The IEEE Council on Electronic Design Automation (CEDA) invites nominations for CEDA Distinguished Lecturers (DLs). The DL Program is an outreach program of CEDA that brings distinguished speakers from academia and industry to give presentations to CEDA chapters, events, and industries in a variety of venues and formats. The DLs are selected and announced in April after approval by the CEDA EC.

Nominees must meet the following criteria:

- The DL nominee must be nominated by a CEDA member who does not have conflict with the selection process. No self-nomination is allowed.
- If you are looking for a nominator we encourage you to contact the chair of your corresponding CEDA Local Chapter.
- The DL nominee must be a well-recognized expert in his/her field because of his/her research, teaching, service activities and an inspiring speaker.

The Distinguished Lecturers will start their two-year term in April. Each Lecturer should submit up to three lecture topics in his/her field of expertise that will be posted on the CEDA website. The Distinguished Lecturers should be readily available to travel within his/her geographical area upon contact by the Chapters or appropriate organizations. Please return a completed nomination form to the CEDA DLP Manager, Tsung-Yi Ho by 18 March 2019. Further information can be found here.

ASAP 2019 – Call for Contributions

The history of the event traces back to the International Workshop on Systolic Arrays, organized in 1986 in Oxford, UK. It later developed into the International Conference on Application Specific Array Processors (ASAP). With its current title, it was organized for the first time in Chicago, USA in 1996. Since then it has alternated between Europe and North-America. The conference will cover the theory and practice of application-specific systems, architectures, and processors. The 2019 conference will take place 15-17 July 2019 at Cornell Tech, NY, USA and will build upon traditional strengths in areas such as computer arithmetic, cryptography, compression, signal and image processing, network processing, reconfigurable computing, application-specific instruction-set processors, and hardware accelerators. The deadline for abstract submission is on 2 April 2019. More information can be found here.

NOCS 2019 – Call for Contributions

The International Symposium on Networks-on-Chip (NOCS) will take place 17-18 October 2019 in New York and will be co-located with the Embedded Systems Week. NOCS is the premier event dedicated to interdisciplinary research on on-chip, package-scale, chip-to-chip, and datacenter rack-scale communication technology, architecture, design methods, applications and systems. NOCS brings together scientists and engineers working on network-on-chip (NoC) innovations and applications from inter-related research communities, including discrete optimization and algorithms, computer architecture, networking, circuits and systems, packaging, embedded systems, and design automation. Topics of interest include but are

not limited to: NoC Architecture and Implementation, Communication Analysis, Optimization & Verification, Novel NoC Technologies, NoC for Intelligent Physical Systems, NoC at the Un-Core and System-level, Inter/Intra-Chip, and Rack-Scale Network.

Electronic paper submission requires a full paper, up to 8 double-column ACM (sigconf) format pages, including figures and references.

A percentage of accepted papers will be recommended for publication in an IEEE journal after revision according to the reviewers' comments. Please find the detailed submission instructions for paper submission, special session, and demo proposals at the submission webpage. The deadline for abstract submission is 10 May 2019.

IEEE JxCDC – Special Issue on Ferroelectric Transistors

With recent advancements in the growth and processing of ferroelectric materials and the emergence of CMOS compatible ferroelectrics, major research and development efforts are underway on ferroelectric transistors for logic, analog, and memory applications. With CMOS scaling facing challenges in improving energy efficiency and power density, research in this area is needed to augment the CMOS technology by lowering the required supply voltage or adding new features and functionalities, such as non-volatility or reconfigurability. Ferroelectric transistors also show great promise for non-traditional circuits, such as convolutional and spiking neural networks and in-memory computing. Research in this area spans many levels of abstraction: from fundamental physical properties and material processing and characterization, to various device concepts, and to circuit and system design and benchmarking.

This special issue of the IEEE JXCDC will present the most recent developments in the area of ferroelectric transistors based on experiments and theoretical models. It aims to feature original papers on various aspects of this emerging technology, its challenges and opportunities, its intrinsic versus practical limits, and the circuits and systems it may enable. The deadline for submissions is 30 April 2019.

ISLPED 2019 – Call for Contributions

The International Symposium on Low Power Electronics and Design (ISLPED) will take place 29-31 July 2019 in Lausanne, Switzerland. ISLPED is a forum for presentation of innovative research in all aspects of low power electronics and design, ranging from process technologies and analog/digital circuits, simulation and synthesis tools, system-level design and optimization, to system software and applications. The conference features regular papers and posters, three keynote presentations, and an industry reception. It also comprises a Design Contest with live demos which encourages submissions from both academia and industry. The submission deadline for abstracts is 4 March 2019. Further information and submission guidelines can be found here.

Papers in IEEE Embedded Systems Letters

The top-five accessed articles from *IEEE Embedded Systems Letters* in January 2019 were as follows:

- "Partitioning Real-Time Tasks With Replications on Multiprocessor Embedded Systems," by J. D. Lin, A. M. K. Cheng, and G. Gercek
- "Multipliers With Approximate 4–2 Compressors and Error Recovery Modules," by M. Ha and S. Lee
- "A 64 kB Approximate SRAM Architecture for Low-Power Video Applications," S. Ataei and J. E. Stine
- "Embedding Encryption and Machine Learning Intrusion Prevention Systems on Programmable Logic Controllers," by T. Alves, R. Das, and T. Morris
- "Tactics to Directly Map CNN Graphs on Embedded FPGAs," by K. Abdelouahab, M. Pelcat, J. Sérot, C. Bourrasset, and F. Berry

Find us online at ieee-ceda.org.

***IEEE Embedded Systems Letters* is open for submissions.**
Visit ieee-ceda.org/publication/esl-publication/author-guidelines.

***IEEE Design & Test* is open for submissions.**
Visit ieee-ceda.org/publication/ieee-design-test-dt/paper-submission-instructions.

CEDA Currents is a publication of IEEE CEDA. Please send contributions to Vasilis F. Pavlidis (contribution form)