



**T**his issue reports on recent EDA activities and looks forward to welcoming upcoming events with the support of CEDA.

### ***EDAthon 2019 at the Chinese University of Hong Kong***

EDAthon 2019 was held successfully on 26 July 2019 with 18 teams coming from universities across mainland China, Hong Kong, and Taiwan. During the one-day competition, all participants exercised their sophisticated coding and analytical skills to solve interesting EDA problems. The three teams were awarded for their outstanding performance as follows:

**Champion:** Peng Zou and Zhipeng Huang (Supervised by Prof. Jianli Chen), Fuzhou University, China;

**Second Place:** Hongzheng Chen and Jiawei Feng (Supervised by Prof. Minghua Shen), Sun Yat-sen University, China; and,

**Third Place:** Mengke Ge and Junpeng Wang (Supervised by Prof. Song Chen), University of Science and Technology of China, China.

EDAthon is one of the major events organized by IEEE CEDA Hong Kong and sponsored by IEEE CEDA. It is a full-day programming contest (9:00am-3:00pm programming + 3:30pm-4:30pm seminar) that features interesting and challenging topics in Electronic Design Automation. This year, we also obtained the industry sponsorship from Cadence, Inc.

### ***Great Success for the 1st Workshop on Machine Learning for CAD (MLCAD)***

The first ACM/IEEE Workshop on Machine Learning for CAD was held on September 2-4, 2020 in Canmore, Alberta, Canada. The location at the entrance to Banff National Park maintained a long tradition of mountain locations for technical meetings. The workshop welcomed 52 participants including eight graduate students. The program committee was co-chaired by Hussam Amrouch of Karlsruhe Institute of Technology and Bei Yu of Chinese University of Hong Kong. The program in-

cluded 30 contributed presentations based on submissions to the program committee as well as five invited talks. The program included talks from both industry and academia; participants were based in Asia, Europe, and North America. The program provided time for in-depth discussion; topics included appropriate types of machine learning methods for various types of CAD problems and challenges associated with training data.

### ***CEDA Brazil Chapter Activities During Chip in Sampa 2019***

The last week of August was intense for the CEDA Brazil Chapter. Three activities were organized in the frame of the [Chip in Sampa 2019](#) event that took place in Sao Paulo. *Chip in Sampa* is the fantasy name that was given to this year's edition of the most important ensemble of symposia and workshops related to microelectronics and embedded systems taking place each year in Brazil. Among those scientific events is SBCCI (the Symposium on Integrated Circuits and Systems Design), which is technically sponsored by CEDA. The total audience of Chip in Sampa reached almost 400 people, which included researchers from academia and industry, students, and entrepreneurs.

The Chip in Sampa technical program included the participation of Dr. Sachin Sapatnekar; made possible thanks to the support of CEDA's Distinguished Lecturer Program. On August 27, Dr. Sapatnekar gave one of the four SBCCI 2019 tutorials entitled "Reliability, Error-resilience, and Approximation in Integrated Systems". The following day, Dr. Sapatnekar gave one of the three keynote talks of Chip in Sampa. The talk entitled "Spintronics: From Devices to Circuits to Systems," was followed by interaction with a large, enthusiastic audience that posed several questions.

Besides the technical activities, Chip in Sampa also hosted the CEDA Brazil Chapter annual meeting. In the meeting, the executive committee reported the activities of the previous 12 months and presented the planned activities for the next months. In the sequel, some new actions were proposed and discussed aiming to reach a

larger number of students in Brazil. Among those, the most relevant is the “CEDA Brazil Talks”, to be organized in cooperation with the Brazilian Computer Society (SBC).

### ***EDA Competition at SMACD 2019***

An EDA competition sponsored by IEEE CEDA, and chaired by Engin Afacan (Kocaeli University) and Fabio Passos (Instituto de Telecomunicações), took place during SMACD 2019 in Lausanne, Switzerland, July 15-18. The SMACD EDA Competition was a thrilling event where students had to compete with their best ideas, methodologies, flows and tools aimed at improving design automation for integrated circuits and systems. The competition required the submission of a full paper, and a presentation at the conference coupled with a live demonstration by the first author, who had to be a MSC or PhD student. The presenter also had to answer the questions from the judging committee, which was formed by experts from industry and academia: David Atienza, EPFL (current president of IEEE CEDA); Elena Blokhina, University College Dublin; Anton Klotz, Cadence; and Marco Cerchi, AMS. This committee had to evaluate papers, presentations, and tools according to the complexity of the problem, level of automation, applicability of the proposal, integration with existing tools and methodologies, and robustness of the design solutions.

Fourteen proposals were submitted and competed for the awards, which included a monetary award of \$1,000, provided by IEEE CEDA, for first place. **The awarded contributions and presenters were:** “Mixed-Signal Hardware Security Using MixLock: Demonstration in an Audio Application”, Julian Leonhard, Sorbonne Université (**second place**) and “TiDeVa: A Toolbox for the Automated and Robust Analysis of Time-Dependent Variability at Transistor Level”, Pablo Saraza-Canflanca, Instituto de Microelectronica de Sevilla (**first place**).

### ***Release of New Robust Design Flow at IC-CAD 2019***

The IEEE CEDA Design Automation Technical Committee (DATC) has developed an open reference design

flow, called DATC Robust Design Flow (RDF), to facilitate research on flow-scale methodology and cross-stage optimizations.

The latest RDF-2019 development, scheduled to be released at ICCAD’19, makes a significant revision of the previously-reported RDF-2018 flow.

Leveraging recent academic tool developments made in the [OpenROAD project](#), RDF-2019 adds previously-missing steps such as floorplanning, I/O placement, power planning, and clock tree synthesis.

A number of horizontal extensions to RDF are also achieved by incorporating additional tool options at the static timing analysis, global placement, gate sizing, and detailed routing stages of the flow.

Additionally, RDF-2019 provides significantly enhanced support of, and interoperability with, industry-standard tools and design formats (LEF/DEF, SPEF, Liberty, SDC, etc.).

Check out the official Github repository of [IEEE CEDA DATC](#).

### ***NOCS 2019 – Call for Participation***

The International Symposium on Networks-on-Chip (NOCS) (Oct 17-18, 2019), is the premier event dedicated to interdisciplinary research on on-chip, package-scale, chip-to-chip, and datacenter rack-scale communication technology, architecture, design methods, applications and systems. NOCS brings together scientists and engineers working on NoC innovations and applications from inter-related research communities, including discrete optimization and algorithms, computer architecture, networking, circuits and systems, packaging, embedded systems, and design automation.

Registration for NOCS 2019 is open at: <https://esweek.org/registration>.

The conference program includes several keynotes, tutorials, special sessions and regular paper session with participants from industry and academia. We hope you are able to attend!

Find us online at [ieee-ceda.org](http://ieee-ceda.org).

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