Currents

January 2019

IEEE Council on Electronic Design Automation

A Word from the President: The Next Challenges for CEDA in 2019: Open Access and Elections Process Definition

Dear Members of our Academic and Industrial Community:

First of all, I would like to wish you all a great New Year 2019 and offer special congratulations to the five newly-elevated IEEE CEDA proposed Fellows as of January 2019. CEDA has reached now 13 years of history and this consistent number of elevated fellows (with 29 elevated fellows in the last five years, by far the largest for any IEEE Council, and even higher than several IEEE societies in this period) is a recognition to its high-quality commitment. Therefore, in 2019 we will target to consolidate CEDA's reputation by strengthening the services and coverage to the EDA and embedded systems community.

During its first year of service, the new Executive Committee (EC) worked really hard in 2018 to increase the support of CEDA to new conferences as well as students and young professionals' activities. In particular, the CEDA EC has increasingly supported the number of activities in local chapters by developing further the CEDA Distinguished Lecturers Program (DLP), sponsoring Luncheon Keynotes and PhD Forum activities, as well as providing travel grants to young researchers from developing countries to present their works at major CEDA sponsored conferences, summer schools and events developed by local chapters. In 2019, we will reinforce these efforts by creating a new global CEDA Student Travel Grant Program that will allow any young researcher (especially from developing regions world-wide) to apply for EC's support to attend and present their work at any CEDA-sponsored conference or event.

In addition, in 2018 CEDA strongly supported the visibility of the community by promoting special issues in CEDA's flagship journal (T-CAD), and magazine (D&T) in the new areas of Internet of Things (IoT), bio-electronic systems design, and new methodologies to conceive nano-technology based devices. All of these areas will be reinforced in 2019 with the consolidation of the CEDA EC publication exploring the option to become fully Open Access Gold in IEEE, as well as creating activities (workshops, special sessions, etc.) jointly with related IEEE societies (e.g., Power Electronics, Computer, Circuits and Systems, Solid State Circuits, etc.) that indicated the interest to work with CEDA on these new topics.

Last, but not least, given the concept of "affiliates" that IEEE has recently created to allow IEEE members to associate with Councils (which cannot have "members"), CEDA currently boasts more than 4,000 affiliates. This is a great achievement for an IEEE Council, but more importantly, this concept of affiliates has prompted the CEDA EC to launch the process of creating ballots and formal open elections to aid in its selection of future EC officers. Thus, in 2019, the current CEDA EC will target establishing this new "open process" for any IEEE member already affiliated with CEDA, to submit a self-nomination, possibly resulting in the opportunity to shape the future of CEDA as a CEDA EC member. Therefore, please keep an eye on our announcements on the CEDA website, CEDA emails, and the CEDA *Currents* for the development of these exciting topics for 2019!

***David Atienza**, IEEE CEDA President*

IEEE Awards Noyce Medal to Antun Domic

The 2019 IEEE Robert N. Noyce Medal will be presented to Dr. Antun Domic, Chief Technology Officer of Synopsys at the annual IEEE Honors Ceremony. The Medal was established in 1999 in honor of Robert N. Noyce, founder of Intel Corporation and inventor of the integrated circuit, to recognize exceptional contributors to the microelectronic industry. This is only the second time in twenty years that the Medal goes to EDA.

Antun received his BS (Licenciatura) in Mathematics & EE from the University of Chile, Santiago, Chile, in 1972, and his Ph.D. in Mathematics from the Massachusetts Institute of Technology, Cambridge, MA, in 1978. He has served, in various capacities, in the technical and executive committees of several IEEE conferences. Antun is currently an EE292A Lecturer at Stanford University, Palo Alto, CA.

Antun started his career in 1978, as a Professor at the Universidad Tecnica del Estado in Santiago, Chile. In 1982 he became a member of the technical staff of MIT Lincoln Laboratories. Antun joined Digital Equipment Corporation in 1985, where he led part of the in-house EDA platform used to design the world's fastest and most complex 64-bit RISC processor at the time, the Alpha 21064: 1.7 M transistors implemented in 750 nm CMOS, running at 200 MHz

After leaving DEC in 1994, Antun worked at Cadence Design Systems, where he led the logic synthesis and place-and-route products and initiated what would become a lifetime mission: to connect logical and physical design, historically separated and mathematically different.

Antun joined Synopsys in 1997 as vice-president of engineering for the Design Tools Group, and progressively expanded his responsibilities. Under his leadership, Synopsys R&D developed and deployed the world first physical synthesis solution in 1999. For the first time, it was possible to thoroughly optimize the gate-level netlist to deal with physical constraints generated by a front-end floor-planner, and yet prove its equivalence against the original netlist or RTL. Chip-level static timing analysis replaced timing simulation and proprietary delay calculators, enabling reliable sign-off of larger and larger chips. RC extraction replaced wire-length back-annotation, further improving sign-off accuracy. The modern RTL-to-GDSII was born.

At the end of 2016, in recognition of his contributions, Antun was appointed Synopsys CTO.

ISLPED 2019 – Call for Contributions

The ISLPED conference is a forum for presentation of innovative research in all aspects of low power electronics and design, ranging from process technologies and analog/digital circuits, simulation and synthesis tools, system-level design and optimization, to system software and applications. The 2019 edition of the conference will be held at EPFL in Lausanne, Switzerland from July 29-31, 2019. The conference features regular papers and posters, three keynote presentations and an industry reception. It also comprises a Design Contest with live demos which encourages submissions from both academia and industry.

Paper abstract registration is until February 25th, 2019. The full paper is due on March 4th, 2019. The design contest accepts submissions until May 3rd, 2019. More information can be found here.

IOLTS 2019 – Call for Contributions

Issues related to On-line testing techniques, and more generally to design for robustness, are increasingly important in modern electronic systems. In particular, the huge complexity of electronic systems has led to growth in reliability needs in several application domains as well as pressure for low cost products. There is a corresponding increasing demand for cost-effective design for robustness techniques. These needs have increased dramatically with the introduction of nanometer technologies, which impact adversely noise margins; process, voltage and temperature variations; aging and wear-out; soft error and EMI sensitivity; power density and heating; and make mandatory the use of design for robustness techniques for extending, yield, reliability, and lifetime of modern SoCs. Design for reliability becomes also mandatory for reducing power dissipation, as voltage reduction, often used to reduce power, strongly affects reliability by reducing noise margins and thus the sensitivity to soft-errors and EMI, and by increasing circuit delays and thus the severity of timing faults. There is also a strong relation between Design for Reliability and Design for Security, as security attacks are often fault-based. The International Symposium on On-Line Testing and Robust System Design (IOLTS) is an established forum for presenting novel ideas and experimental data on these areas. The Symposium is sponsored by the IEEE Council on Electronic Design Automation (CEDA) and the 2019 edition is organized by the IEEE Computer Society Test Technology Technical Council, the University of Athens, and the TIMA Laboratory. All submission information and topic details can be found here.

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