Call for Papers: IEEE JxCDC

The IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (JxCDC), an open access only publication, calls for papers on the Special Topic on Tunneling FETs for Energy-Efficient Computing & Information Processing. This special issue is organized by Dr. Uygar Avci and Prof. Azad Naeemi.

The Tunneling Field-Effect Transistor (T-FET) is considered a future transistor option due to its steep-slope prospects and the resulting advantages in operating at low supply voltage (V_{DD}). Reducing supply voltage (V_{DD}) while keeping a low leakage current and a reasonably high on-current is critical for minimizing energy consumption and improving the energy efficiency of computing and information processing. The thermal limit (Boltzmann's Tyranny) of the MOSFET transistor subthreshold swing (SS) restricts lowering its threshold voltage (V_t), causing significant performance degradation at low V_{DD}. A Tunneling Field Effect Transistor's (T-FET) SS is not limited by this thermal tail and may perform better at low V_{DD}.

This call for papers on Tunneling FETs is for rapid publication of seminal results across the areas of T-FET materials, devices, and circuits for novel computation and information processing paradigms. Paper submissions with key insights into the advantages and challenges of specific T-FET device and material designs and circuit techniques are especially valued in order to guide the semiconductor industry and academia on a path toward more energy-efficient computing.

Topics of interest include:

- N- and P- Tunneling FET experimental transistors demonstrating high performance at low supply voltage
- T-FET material and device design, including hetero-junction III-V materials, transition metal dichalcogenides, other two-dimensional materials and their hetero-junctions
- T-FET circuits for energy efficient computing and information processing
- Energy-Efficient computing and information processing with T-FET transistor circuits and architectures.

Submission guidelines and a paper template are provided here. The submission deadline is **June 30, 2020**.

Call for Papers: IEEE Transactions on Computers

This call for papers is for a special issue on Smart Edge Computing and IoT, organized by Prof. Luca Benini, Prof. Taekwang Jang, Dr. Abbas Rahimi, and Dr. Simone Benatti.

The evolution of the Internet-of-Things (IoT) is changing the nature of edge-computing devices. End-nodes have to support, in-place, an increasing range of functionality: multi-sensory data processing and analysis, complex systems control strategies and, ultimately, artificial intelligence. These new capabilities will enable disruptive innovation in wearable and implantable biomedical devices, autonomous insect-sized drones, autonomous smart environmental sensing, safety-critical real-time applications and structural health monitoring, and more. In this special issue, we are seeking contributions on IoT Smart Edge Computing Architectures, Systems and related hardware-software design approaches.

Topics of interest include, but are not limited to:

- Hardware-software design approaches for smart edge processing
- Heterogeneous systems-on-chip and architecture for energy efficient smart edge processing
- Low power analog and mixed signal computing, in-memory computing, in-sensor computing
- Edge machine-learning architectures dealing with sensor and signal variabilities
- Neuro-symbolic, brain- and bio-inspired computing paradigms for edge processing
- IO and peripherals for energy efficient interfaces in edge computing system
- Edge processing for biomedical IoT systems and human machine interaction
- Smart edge IoT devices for structural health monitoring and predictive maintenance
- Real-time and safety-critical smart edge sensors for industrial IoT

Submissions to this special section must represent original material that has been neither submitted to, nor published in, any other journal. Articles should be submitted here by selecting the aforementioned special issue. The submission deadline is **August 30, 2020**.

6th IEEE International Smart Cities Conference – IEEE ISC2 2020

The 6th IEEE International Smart Cities Conference (ISC2 2020) will be held as a virtual conference, from September 28 – October 1, 2020. The worldwide governmental restrictions on travel, gatherings, and meetings, imposed to limit and slow the spread of the novel coronavirus, make it impossible to organize the conference in the traditional format. However, we are confident that the changes induced by the virus to our everyday lives, and the responses given to these new challenges by smart city researchers and practitioners, city policymakers and administrators, critical infrastructure operators and industry representatives, economists and sociologists will generate exciting and edifying presentations and discussions, both as part of our keynote addresses, panel debates, workshops or research talks. After all, one of the main reasons for cities becoming smart should be to safely and efficiently support us, citizens, in such difficult times. The theme of the conference this year is: Smart Cities Solutions for New Challenges, Including a Pandemic.

Besides contributions addressing the conference theme, authors are welcome to submit their original research results in traditional topics across broad application and functional domains, within the context of smart urban infrastructure systems. The technical areas include, but are not limited to:

- Community & Governance
- Infrastructure & Technology
- Data, Privacy, & Security

For detailed submission instructions and related submission deadlines, visit the conference website. The submission deadline for regular papers is **July 1, 2020**.

Call for Papers ASP-DAC 2021

ASP-DAC 2021 is the 26th annual international conference on VLSI design automation in Asia and South Pacific regions, one of the most active regions of design and fabrication of silicon chips in the world. This edition of ASP-DAC will take place between January 18-21, 2021, at Miraikan, Tokyo, Japan.

The conference aims at providing the Asian and South Pacific CAD/DA and Design community with opportunities of presenting recent advances and with forums for future directions in technologies related to Electronic Design Automation (EDA). The format of the meeting intends to cultivate and promote an instructive and productive interchange of ideas among EDA researchers/developers and system/circuit/device designers. All scientists, engineers, and students who are interested in theoretical and practical aspects of VLSI design and design automation are welcomed to ASP-DAC.

In light of the continued Covid-19 pandemic situation, the format of the conference is subject to future change. The options include fully in-person conference, hybrid conference (in person plus live video presentation) and fully virtual conferences. All papers presented, whether in-person or online, will be published. Please check the ASP-DAC 2021 website for updates. For detailed submission instructions, please refer to this link. The submission deadline is **July 26, 2020**.

Design Automation WebiNars (DAWN)

The first DAWN on the topic of Machine Learning for EDA took place on May 7, 2020. It was composed of five excellent talks followed by Q&A with the panellists. The event was successfully organized by Professors Yiran Chen, Duke University, and Tsung-Yi Ho, National Tsing Hua University. The video recording of this webinar can be found to CEDA's website at this link.

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