



IEEE Council on Electronic Design Automation

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2016 CAD Contest at ICCAD

The CAD contest at ICCAD is among the premier research and development contests in the field of Electronic Design Automation (EDA). Since its inaugural year of 2012, the CAD contest at ICCAD has been a worldwide competition, conducted with joint sponsorship from IEEE CEDA and the Ministry of Education, Taiwan. In addition, in this year, the contest also received the financial sponsorship from the industry, including Synopsys Taiwan Co., Ltd., Taiwan, Cadence Design Systems Inc., Taiwan, and MediaTek, Inc., Taiwan.

Over the years, the CAD contest at ICCAD has presented challenging problems in varied topic areas, such as, logic synthesis, physical design, design for manufacturability, and 3D IC design. Together with the associated real-world benchmarks and common evaluation frameworks, the contest problems have played a key role in advancing the state-of-the-art in EDA. Additionally, they have fostered productive industry-academia collaboration. In the past four years, the contest has witnessed a progressive increase in worldwide participation: 56 teams from 7 countries/regions in 2012, 87 teams from 9 countries/regions in 2013, 93 teams from 9 countries/regions in 2014, and 112 teams from 12 countries/regions in 2015. Thus far, it has led to more than 95 publications in

top-tier conferences and journals, which have undoubtedly boosted EDA research and extended the impact of the contest.

Continuing the rich tradition, the 2016 CAD Contest at ICCAD attracted 135 multi-person teams from 11 countries/regions, including Taiwan, Mainland China, Hong Kong, Korea, India, Iran, Japan, Canada, USA, Brazil, and Russian Federation. In total, these teams comprised of 317 students and 62 professors. Contestants participated in one or more problems in the three topic areas of (a) design verification, (b) logic synthesis, and (c) design for Manufacturing. Along with the release of the contest benchmarks, the contest results were announced at ICCAD 2016, held from November 7-10 at Austin, Texas. The contest problems and final results are summarized as follows.

The first topic addressed the problem of identical fault search. Injecting faults into designs is a way to qualify a verification environment. To improve the performance of the qualifying process, identical faults should be removed. In this problem, the contestants were expected to identify all sets of identical faults. The evaluation was based on the correctness, the execution time and the memory usage. The winners were: Dao Ai Quoc, Prof. Mark Po-Hung Lin, Dr. Alan Mishchenko – National Chung Cheng University, Taiwan

The second topic addressed the problem of non-exact Projective NPNP boolean matching. Basic boolean matching is for NPNP-equivalence, which negates (N) and permutes (P) circuit inputs and outputs to achieve circuit equivalences. The objective of this problem is to develop a more flexible and powerful boolean matching engine that can be widely utilized in industry tools. The winners were: Chak-Wa Pui, Peishan Tu, Haocheng Li,

Gengjie Chen, Prof. Evangeline F.Y. Young – The Chinese University of Hong Kong, Hong Kong

The third topic addressed the problem of pattern classification for integrated circuit design space analysis. Given a circuit layout and various markers, contestants are asked to provide a reduced set of representative layout clips around these markers. Each such representative clip identifies a class and has an associated set of one or more unique layout markers. Speed and accuracy are key aspects to target in the solutions. The winners were: Mehmet M Isgenc, Joseph Sweeney, Samuel Pagliarini, Mayler Martins, Prof. Larry Pileggi – Carnegie Mellon University, USA

The problems, associated benchmark suites, and final results are available at the official contest website: <http://cad-contest-2016.el.cycu.edu.tw/CAD-contest-at-ICCAD2016/index.html>. Please keep your eyes open for publications that are driven by the 2016 CAD contest in upcoming conferences and journal editions.

You are invited to participate in the 2017 CAD contest at ICCAD!

Papers in IEEE Embedded Systems Letters

The top-five accessed articles from *IEEE Embedded Systems Letters* in November 2016 were as follows:

- “[Energy Efficient Outdoor Light Monitoring and Control Architecture Using Embedded System](#),” by Z. Kaleem, T.M. Yoon, and C. Lee
- “[Partitioning Real-Time Tasks With Replications on Multiprocessor Embedded Systems](#),” by J. Denny Lin, A. M. K. Cheng, and G. Gercek
- “[Arduino Debugger](#),” by J. Dolinay, P. Dostálek, and V. Vasek

- “[Improving Dynamic Memory Allocation on Many-Core Embedded Systems With Distributed Shared Memory](#),” by I. Koutras et al.
- “[A Compact Portable Microwave Life-Detection Device for Finding Survivors](#),” by F. JalaliBidgoli, S. Moghadami, and S. Ardalan

Papers in IEEE Design and Test

The top-five accessed articles from *IEEE Design and Test* in November 2016 were as follows:

- “[In Vitro Long-Term Performance Evaluation and Improvement in the Response Time of CMOS-Based Implantable Glucose Sensors](#),” by T. Tokuda et al.
- “[Approximate Computing: A Survey](#),” by Q. Xu, T. Mytkowicz, and N.S. Kim
- “[Cybersecurity for Control Systems: A Process-Aware Perspective](#),” by F. Khorrami, P. Krishnamurthy, and R. Karri
- “[The Changing Computing Paradigm With Internet of Things: A Tutorial Introduction](#),” by S. Ray, Y. Jin, and A. Raychowdhury
- “[Ultralow Power and the New Era of Not-So-VLSI](#),” by M. Wolf

Upcoming Conferences (Yao-Wen Chang, conferences@ieee-ceda.com)	
DATE	Lausanne, Switzerland, 27-31 March 2017
GLSVLSI	Alberta, Canada, 10-12 May 2017
WIE ILC	San Jose, California, 22-23 May 2017
ETS '17	Limassol, Cyprus, 22-26 May 2017
DAC	Austin, Texas, 18-22 June 2017

Find us online at <http://ieee-ceda.org>.



IEEE Embedded Systems Letters is open for submissions. Visit mc.manuscriptcentral.com/les-ieee.

IEEE Design & Test is open for submissions. Visit mc.manuscriptcentral.com/dandt and ieee-ceda.org/publications/d-t/paper-submission.

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CEDA Currents is a publication of IEEE CEDA. Please send contributions to Jose L. Ayala (jayala@fdi.ucm.es).

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