May 2013

Currents

IEEE Council on Electronic Design Automation

Presenting DAC 2013

The Design Automation Conference (DAC), held 2-6 June 2013 in Austin, Texas, is celebrating 50 years as the leading technical conference and tradeshow on electronic design, design automation, embedded systems, and software.

DAC 2013 hosts more than 300 presentations, consisting of technical sessions, panels, exciting keynotes, tutorials, workshops, and collocated events covering the latest in design methodologies, embedded software, and EDA tool developments. This year's conference features keynotes by speakers from National Instruments, Samsung, Freescale Semiconductor, Texas Instruments, and Qualcomm. An exciting addition to this year's program is the Designer Track, featuring 20 invited speakers from senior designers, tech leads, and managers.

The exhibition offers more than 175 of the leading EDA, IP, embedded systems, and design service providers, along with the ARM Connected Community Pavilion. Conference details are available at http://www.dac.com.

CAD Contest at ICCAD

Contests and their benchmarks, such as those at the International Symposium on Physical Design (ISPD) and the Design Automation Conference (DAC), have become an important driving force in pushing the EDA domain forward in different areas. To encourage better research development on timely and practical EDA problems across all domains, a new CAD contest was held in 2012, under the joint sponsorship of IEEE CEDA and the Taiwan Ministry of Education. The contest took place at the 2012 IEEE/ACM International Conference on Computer-Aided Design (ICCAD). The contest's predecessor was the annual CAD Contest in Taiwan, which had been held for 12 consecutive years.

The CAD contest generally comprises problems contributed by EDA vendors (Cadence Design Systems, Synopsys, SpringSoft), IC and IP design houses (Faraday Technology, Global UniChip), and research institutes (Industrial Technology Research Institute, CIC). More than 100 teams have participated in this contest annually. Nearly half of all registered teams consist of undergraduate students from electrical engineering, computer science, and mathematics departments.

Through the process of theoretical development and practical implementation, the contest has attracted many undergraduate contestants to get involved in further EDA research for their graduate studies. In addition, the winning teams often publish their techniques and results in leading journals or conferences. Most of the winners have further pursued careers in the EDA area as faculty members, researchers, or engineers at top-tier companies. Over its history, the CAD contest has made significant contributions to popularizing EDA education and boosting EDA research momentum in Taiwan.

In the first year of the new cooperation between CEDA and the Taiwan Ministry of Education, the 2012 CAD contest attracted 56 teams from seven regions, including the US, Japan, China, Hong Kong, Korea, Italy, and Taiwan. In total, 145 students and 59 professors participated.

Three representative critical problems on functional engineering change order (ECO) (logic synthesis and verification), routability-driven placement (physical design), and lithographic hot-spot detection (design for manufacturability) were designed and run by industry experts from Cadence Design Systems, IBM Research, and Mentor Graphics.

Topic chair Jane Wang (Cadence Design Systems) managed the first contest problem, on logic difference extraction for functional ECO. First place went to "HillWalker," by Yu-Liang Wu (Chinese University in Hong Kong) and his students Xing Wei, Yi Diao, and Tak-Kei Lam. Second place went to "TTLABNOONE," by the team of TingTing Hwang (National Tsing Hua University). Third place went to "dvlab," by the lab of Chung-Yang (Ric) Huang (National Taiwan University).

Topic chair Natarajan Viswanathan (IBM Austin Research Laboratory) managed the second contest problem, on design hierarchy and global routing congestion at placement. First place went to "SimPLR," by Igor Markov (University of Michigan) and his students

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Myung-Chul Kim and Jin Hu. Second place went to "RippleCUHK," by the team of Evangeline Young (Chinese University in Hong Kong). Third place went to "NTUplace4h," by the lab of Yao-Wen Chang (National Taiwan University).

Topic chair J. Andres Torres (Mentor Graphics) managed the third contest problem, on fuzzy pattern matching for lithography hot-spot detection. First place went to "Iris' Excalibur," by Geng-He Lin and Yen-Ting Yu (National Chiao Tung University). Second place went to "UTDetector," by David Z. Pan (University of Texas at Austin) and his team. Third place went to "Extinguisher," by the lab of Yao-Wen Chang (National Taiwan University).

In addition, a new set of industry benchmarks for each contest problem was released. These benchmarks are expected to help push the advancement of related research.

Many of the participants in this CAD contest have prepared conference papers on the research related to their contest submissions, with the first appearing at DAC 2013. We also expect journal articles to appear in the future. The momentum from these publications should boost related research and extend the impact of this contest.

Preparation for the 2013 CAD Contest at ICCAD is ongoing. Details about the contest are available at http://cad_contest.cs.nctu.edu.tw/CAD-contest-at-ICCAD2013. You are invited to participate.

Yih-Lang Li, Iris Hui-Ru Jiang, and Zhuo Li (contest co-chairs)

TCAD Donald O. Pederson Best Paper Award

The TCAD Donald O. Pederson Best Paper Award honors an outstanding technical contribution that has appeared in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (*TCAD*) in the preceding two calendar years. The 2013 award goes to Wangyang Zhang, Xin Li, Frank Liu, Emrah Acar, Rob A. Rutenbar, and Ronald D. (Shawn) Blanton for their paper, "Virtual Probe: A Statistical Framework for Low-Cost Silicon Characterization of Nanoscale Integrated Circuits," which appeared in Dec. 2011 *TCAD*.

This paper addresses the problem of measuring, characterizing, and monitoring spatially correlated interdie and intradie variations in nanoscale ICs. The virtual probe proposed in this paper leverages new results in compressed sensing to predict on-chip spatial correlations. Using these ideas, the authors show how it is possible to obtain accurate sample results via a sparse set of sensors, with a spatial sampling frequency that is far below the well-known Nyquist rate.

Papers in IEEE Embedded Systems Letters

The top-five accessed articles from *IEEE Embedded Systems Letters* in March 2013 were as follows:

- "Reconfigurable Computing in Next-Generation Automotive Networks," by S. Shreejith, S.A. Fahmy, and M. Lukasiewycz
- "Softcore Processor Optimization according to Real-Time Application Requirements," by B. Le Gal and C. Jego
- "Formal Methods for Early Analysis of Functional Reliability in Component-Based Embedded Applications," by A. Hazra et al.
- "Hardware-Assisted Detection of Malicious Software in Embedded Systems," by M. Rahmatian et al.
- "Wireless Sensor Networks for Pilgrims Tracking," by M. Mohandes et al.

Upcoming Conferences (David Atienza, david.atienza@epfl.ch)	
DAC	Austin, Texas, 2-6 June 2013
MPSoC	Otsu, Japan, 15-19 July 2013
PATMOS	Karlsruhe, Germany, 9-11 Sept. 2013

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IEEE Embedded Systems Letters *is open for submissions. Visit mc.manuscriptcentral.com/les-ieee*

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