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Currents

IEEE Council on Electronic Design Automation

NEW Technical Column: Call for Contributions

CEDA Currents is starting a new technical column, featuring a short note on current developments and news related to design, design methodology, and design automation of electronic circuits. Contributions should be sent to Jose L. Ayala (jayala@ucm.es), CEDA Currents Editor. Submissions should be approximately 200 to 400 words and should include one figure. This figure should be submitted as a separate, high-resolution (300 dpi) file and should not have been published anywhere else (other than in IEEE publications). Suggestions and comments about this column are most welcome.

Adaptive and Resilient Circuits for Dynamic Variation Tolerance

The Dec. 2013 issue of *IEEE Design & Test* (*D&T*) was dedicated to variability and aging of ICs. Variability in device and circuit parameters is one of the primary challenges in the semiconductor industry today. Parameter variations adversely affect the performance and energy efficiency of microprocessors across all market segments, ranging from small embedded cores in SoCs to large multicore servers.

A distinguishing feature of a parameter variation is the temporal characteristic. A *static parameter variation* results from variability in the manufacturing process. A *dynamic parameter variation* occurs during the microprocessor operation as environmental and workload conditions change.

Examples of dynamic parameter variation include supply voltage (V_{CC}) droops, temperature changes, and transistor aging. Conventional designs build in clock frequency (FCLK) or V_{CC} guard bands to ensure correct functionality in the presence of worst-case dynamic variations. Consequently, these inflexible designs cannot exploit the opportunities for higher performance by increasing FCLK, or lower energy by reducing V_{CC}. Most systems usually operate at nominal conditions in which worst-case scenarios rarely occur. So, these necessary guard bands for infrequent dynamic variations severely limit the performance and energy efficiency of conventional microprocessors.

In the *D&T* special issue on variability and aging, the first article describes three distinct circuit techniques for dynamic variation tolerance: traditional on-die monitors and adaptive circuits; resilient error-detection and recovery circuits; and adaptive clock distribution for high-frequency V_{CC} droop tolerance.[1] These three designs mitigate the FCLK and V_{CC} guard bands for dynamic parameter variations to enhance microprocessor performance and energy efficiency while providing unique trade-offs in guard band reduction and overheads.

Although traditional on-die monitors and adaptive circuits incur the least design overhead, this design provides the smallest amount of guard band reduction, primarily resulting from the inability to respond to high-frequency V_{CC} droops. Resilient error-detection and recovery circuits enable the largest magnitude of guard band reduction at the highest cost in design overhead, which requires error recovery for any failure scenario. The adaptive clock distribution aims to retain the low overhead of the traditional adaptive design while reducing the guard band for high-frequency V_{CC} droops. Compared to conventional designs, the 22-nm silicon test-chip measurements of the adaptive clock distribution in Figure 1 demonstrate simultaneous throughput gains and energy reductions ranging from 14% and 3% at 1.0 V to 31% and 15% at 0.6 V, respectively, for a 10% V_{CC} droop.

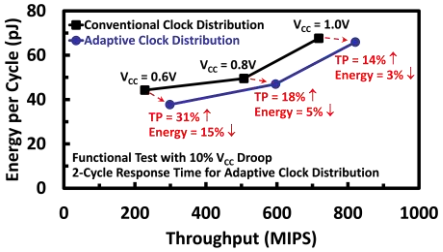

Figure 1. Measured energy per cycle versus throughput for conventional and adaptive clock distributions.[2]

References:

1. K.A. Bowman et al., "Adaptive and Resilient Circuits for Dynamic Variation Tolerance," *IEEE Design & Test*, Dec. 2013, pp. 8-17.
2. K.A. Bowman et al., "A 22 nm All-Digital Dynamically Adaptive Clock Distribution for Supply Voltage Droop Tolerance," *IEEE J. Solid-State Circuits*, Apr. 2013, pp. 907-916.

CEDA Currents is a publication of IEEE CEDA. Please send contributions to Jose L. Ayala (jayala@fdi.ucm.es).

2014 CAV Award Announcement

The Computer-Aided Verification (CAV) Award recognizes a specific fundamental contribution or a series of outstanding contributions to CAV. This year's award (which includes a $10,000 gift) was presented at the 26th Annual CAV Conference to Patrice Godefroid, Doron Peled, Antti Valmari, and Pierre Wolper for their seminal work in developing partial-order-reduction algorithms for efficient state-space exploration of concurrent systems.

Concurrency is present in computer systems at all levels, from concurrent software running over multicore platforms to distributed applications running over large-scale networks. The automated verification of such systems is challenging due to the highly complex interactions between their components. Standard verification algorithms based on systematic state-space exploration face the well-known state-explosion problem when applied to such systems: the size of the state space of concurrent systems grows exponentially in the number of their components.

A major approach for tackling this problem and developing scalable algorithms for automated verification of concurrent systems is to use partial-order reduction (POR) techniques. A huge number of computations often lead to the same observable states (those that are relevant for checking the property under consideration), and differ only in the order in which some parallel actions are interleaved. These actions are actually independent of one another (they are not conflicting), so their total ordering in a particular execution is not relevant. POR techniques consider such computations as equivalent, so that only one representative of each equivalence class needs to be considered during the state-space exploration.

The notion of independence was first formulated in 1977 by Antoni Mazurkiewicz, and has been studied since then in the context of concurrency semantics by several researchers. However, it was not until the first half of the 1990s that these ideas were applied in algorithmic verification.

Although the POR idea seems natural and simple in principle, the difficulty is in designing efficient search algorithms that determine on the fly (during the state-space exploration of the system) which branches to prune and which to explore, while ensuring that redundant explorations are avoided and that the state-space exploration is still complete– that is, no computation equivalence class (modulo reordering of independent actions) is missed.

From 1990 to 1994, Godefroid, Peled, Valmari, and Wolper investigated this problem and defined algorithms for solving it. These algorithms constitute the basis of the POR approach to model checking, which has been subsequently developed further, extended to various system classes, and integrated into several verification methods and tools. These tools are now widely used and applicable in both academia and industry.

POR has been one of the major contributions to the field of automated verification in the past two decades. Its development has contributed in a critical way to making model checking successful and practically applicable to concurrent systems. This success is due in large part to the seminal work that Godefroid, Peled, Valmari, and Wolper did in the first half of the 1990s. With this award, the community recognizes the historical importance and the deep impact of their contribution.

Papers in IEEE Embedded Systems Letters

The top-five accessed articles from *IEEE Embedded Systems Letters* in June 2014 were as follows:

- "An FPGA-Based Plant-on-Chip Platform for Cyber-Physical System Analysis," by S. Vyas et al.
- "A Security Layer for Smartphone-to-Vehicle Communication over Bluetooth," by A. Dardanelli et al.
- "Runtime Adaptation of Applications Using Design of Experiments: A Smartphone-Based Case Study," by F. Maker, R. Amirtharajah, and V. Akella
- "Verilog-A Based Effective Complementary Resistive Switch Model for Simulations and Analysis," by Y. Yang et al.
- "High Communication Throughput on Low Scan Cycle Time with Multi/Many-Core Programmable Logic Controllers," by A. Canedo, H. Ludwig and M.A. Al Faruque

IEEE Embedded Systems Letters ***is open for submissions. Visit mc.manuscriptcentral.com/les-ieee***

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