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Currents

IEEE Council on Electronic Design Automation

Thermal-Aware Floorplanning for 3D MPSoCs

The emergence of heterogeneous many-core architectures presents a unique opportunity for delivering order-of-magnitude performance increases to high-performance computing (HPC) applications by matching certain classes of algorithms to specifically tailored architectures. Specific HPC applications such as *N*-body simulations, molecular dynamics, and terrain rendering can experience order-of-magnitude or greater speedups when paired with architectures that are specifically tailored to their needs. One such example from the HPC community is the Los Alamos National Labs' Roadrunner system.

This trend of executing target applications in many parallel cores is one of the characteristics of current data centers. Moreover, multiprocessor SoCs (MPSoCs) have now reached the category of many-core systems. Intel Labs has created its experimental Single-Chip Cloud Computer (SCC), a research microprocessor containing the most Intel architecture cores ever integrated on a silicon CPU chip: 48 cores. SCC incorporates technologies intended to scale multicore processors to 100 cores and beyond, such as networks on chip (NoCs), advanced power management technologies, and message-passing support.

The exponentially increasing power densities that have been reached in current technologies, the values of leakage currents, the cooling costs, and the recent reliability constraints in microprocessor-based systems have made cooling the chip temperature one of the main concerns in system design. The operating temperature has a significant impact on microprocessor design. At higher temperatures, transistors work more slowly because of the degradation of carrier mobility. The resistivity of the metal interconnects also increases, causing longer delays and, therefore, performance degradation.

To maintain the chip temperature under a certain limit, the hardware module's power density can be decremented by increasing the chip area. However, the high cost and the challenge of meeting all the geometric constraints make this approach unrealistic.

Orthogonal to the functional blocks' power density, another important factor that affects the chip's temperature distribution is the lateral spreading of heat in silicon. This depends on the placement of the units and their proximity to the chip border and other units that behave as thermal sinks or thermal sources.

Thermal-aware floorplanning algorithms can even out the temperatures of the hardware modules by spreading the heat dissipation. This aspect of floorplanning is particularly attractive compared with static external cooling, which reduces the chip surface's temperature by a constant factor (it does not reduce the temperature gradient across the chip).

3D multiprocessor chips have been proposed as an effective mechanism to significantly improve system performance by reducing interconnect delays and increasing the density of the integrated logic, turning the many-core, single-chip concept into a reality. This mechanism also allows the integration of multiple and disparate technologies, such as RF and mixed-signal components.

A major concern in the adoption of 3D architectures is the increased power densities that can result from placing one computational block over another in the multilayered 3D stack. Also, the thermal conductivity of the dielectric layers inserted between device layers for insulation is very low compared to silicon and metal. Because power densities are already a major concern in 2D architectures, the move to 3D architectures will accentuate the thermal problem. Consequently, efficient 3D floorplanning mechanisms must be designed to optimize the thermal profile of these complex 3D multiprocessor architectures.

Our recent research in the area of thermal-aware floorplanning for 3D MPSoCs proposes a mixed-integer linear programming (MILP) formulation and an efficient solver that manages multiple objectives in the minimization problem. We are also exploring a many-core heterogeneous single chip for experimental purposes.

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CEDA Currents is a publication of IEEE CEDA. Please send contributions to Jose L. Ayala (jayala@fdi.ucm.es) or Rajesh Gupta.

Design Automation and Smart Grid II

The Design Automation Technical Committee (DATC) promotes and facilitates the sharing of ideas, techniques, standards, and expertise for more effective use of design automation technology. It also conducts workshops, conferences, and other meetings to advance both the state of the art and the state of the practice in design automation.

A recent initiative of DATC is to venture into smart-grid research as an exploration of the adjacent spaces of design automation. DATC organized the "Workshop on the Synergy between Design Automation and Smart Grid" at the 2010 Design Automation Conference. Based on the success of this workshop, DATC (under the auspices of CEDA) is organizing a follow-up workshop. This workshop will be held 9 June 2011, and will be co-located with the Design Automation Conference in San Diego, California.

The 2010 workshop introduced the design automation and power energy communities to each other, providing a forum for exchanging domain knowledge between the two respective disciplines. The follow-up workshop will further strengthen the ties between the two communities and provide in-depth insights into potential smart-grid topics that the design automation community can work on. The workshop will feature educational sessions, current research presentations from the power energy community, and related smart-grid work from the design automation community.

Topics in the design automation domain may include hybrid-control systems, optimization techniques for stochastic economic dispatch, power system operations, dynamic simulation, and agent-based smart-grid simulation. Topics in the power energy domain may include arena-renewable generation, load forecasting, and demand response. The workshop will also sample selective research topics on the smart grid from design automation researchers who have ventured into the power energy domain. Finally, DATC will host a contest on smart-grid simulation, targeting the design automation community. We look forward to active participation from CEDA members. See you there!

David Kung, DATC chair, kung@us.ibm.com

Papers in IEEE Embedded Systems Letters

The top-five accessed articles from *IEEE Embedded Systems Letters* during December 2010 were as follows:

- "Design of a Low-Cost Underwater Acoustic Modem," by B. Benson et al.
- "Smartphone-Based Vehicle-to-Driver/Environment Interaction System for Motorcycles," by C. Spelta et al.
- "Hierarchical Additive Hough Transform for Lane Detection," by R.K. Satzoda et al.
- "System-Level Energy Optimization for Error-Tolerant Image Compression," by S.H. Kim et al.
- "High-Speed AES Encryptor with Efficient Merging Techniques," by I. Hammad et al.

Upcoming Conferences (Bill Joyner, william.joyner@src.org)	
GLSVLSI	Lausanne, Switzerland, 2-4 May 2011
DAC	San Diego, Calif., 5-10 June 2011
MEMOCODE	Cambridge, UK, 11-13 July 2011
PATMOS	Madrid, 27-30 September 2011
FMCAD	Austin, Texas, 30 Oct.-2 Nov. 2011
VLSI-SoC	Hong Kong, 17-19 Oct. 2011

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