AUGUST 2008

Currents

CEDA

IEEE Council on Electronic Design Automation

CEDA Standards Committee

The Council of EDA Standards Committee (C-EDA SC) is to promote the development of Standards in the EDA industry. Such standards are beneficial to the IC designers and developers and users of automation tools in this industry since they provide a mechanism for defining common semantics. This committee will be represented by EDA, Consortiums, Semiconductor Companies and associated standards groups. The C-EDA SC acts as the administrator for the Working Groups under it which develop and maintain Standards.

The C-EDA SC is governed by a chairman and a steering committee. The steering committee is composed of the chair-persons of the Working Groups under the C-EDA SC plus explicitly voted in members to include senior management in EDA, representatives from consortiums, representative from DASC and/or other interested parties and ex-officio members who may be chosen for the sake of continuity or coordination with related groups. The ex-officio members will also include such functions as are required for the effective administration of the C-EDA SC such as secretary. The ex-officio members will be selected by the steering committee.

Since this committee is just forming things are changing at a very rapid pace. To keep yourself updated, information will be posted on *http://grouper.ieee.org/groups/ceda* .

CEDA has also organized a Panel Session on EDA Standards for the recent EDP Workshop (Monterey, California, April 2008) promoting the initial approaches taken by the Council.

Please contact Rohit Kapur (Rohit.Kapur@synopsys.com) and John Darringer (jad@us.ibm.com) for further information.

Nominations Requested for EDA Industry's Prestigious Kaufman Award

Nominations for this year's recipient of the Phil Kaufman Award for Distinguished Contributions to EDA are being accepted until Monday, June 30. The award will be presented in October at the 15th annual Phil Kaufman Award dinner and ceremony in Santa Clara, California. Dr. Robert K. Brayton, Cadence Distinguished Professor of Electrical Engineering and Computer Science at the University of California at Berkeley, was the 2007 award winner. Prof. Brayton won the Phil Kaufman Award for his demonstrable impact on the field of electronic design through contributions in Electronic Design Automation (EDA).

The Kaufman Award, jointly sponsored by CEDA and the EDA Consortium, honors individuals who have made a demonstrable impact on the field of EDA in business, industry direction and promotion, technology and engineering, or education and mentoring. It was established in 1994 in honor of deceased EDA industry pioneer Phil Kaufman, who turned innovative technologies like silicon compilation and emulation into businesses that have benefited electronic designers.

Please, visit *http://www.edac.org/about_kaufman_award.jsp* or *http://www.ieee-ceda.org/awards.html* to download this year's nomination form.

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Overview: International Conference on Computer Aided Design (ICCAD).

The International Conference on Computer-Aided Design (ICCAD) is the world's premiere conference in electronic design technology and has served EDA and Design professionals for the last 25 years by highlighting new challenges and breakthrough innovative solutions for integrated circuit design technologies and systems. With continued strong participation from around the world, including North America, Europe, and Asia, the ICCAD received nearly 500 technical paper submissions of very high quality. The ICCAD conference will be held on November 10-13 at the DoubleTree Hotel in San Jose, California.

"ICCAD continues to be the premiere and most selective conference devoted to technical innovations in design automation of devices, circuits, and systems," stated Sani Nassif, ICCAD 2008 General Chair. "As the number of conferences and meeting options for professionals and academics continues to grow, ICCAD remains uniquely

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recognized as the place where the most in-depth and respected research work in EDA is presented. This year we are enhancing ICCAD by offering our global set of attendees the option of attending a number of co-located workshops to further drill down in specific areas, and a strong line-up of keynotes that reflects the future of the broader fields of design automation."

Outstanding broadening keynotes

Such progress comes in the wake of a very successful 2007 Program that included two extremely well received keynotes from Jeffrey Welser from the Nano-Electronics Research Initiative and John Kibarian from PDF Solutions.

This year, ICCAD will host Mary Lou Jepsen, founder and CEO of Pixel Qi, and formerly the founding chief technology officer of the iconic One Laptop per Child (OLPC) project. Ms. Jepsen brings a unique perspective of the design of systems in general, and a future vision of the display as computer that will likely drive the future of personal electronics.

Co-located Workshops

As the ICCAD ecosystem broadens, and the need for effective technical conferencing and networking soars in our industry, ICCAD has started an initiative to host a selected number of co-located workshops. These workshops are not only related to the field of automated design, but also of the same caliber as the conference itself, thereby focusing on quality not quantity. The workshops will leverage the entire conference management infrastructure, and allow attendees to add a focused one-day technical activity with a minimum of disruption to travel schedules.

As an example of these co-located workshops, there is one workshop focusing on Compact Variability Modeling. The workshop fills a gap between traditional device-level conferences like the International Electronic Device Meeting (IEDM) and EDA conferences such as ICCAD since it is widely recognized that process variation is emerging as a fundamental challenge to IC design with scaled CMOS technology.

To learn more, please visit the ICCAD website at www.iccad.com .

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Survey on 3D-Silicon Integration

Contributed by Prof. David Atienza (Complutense University of Madrid, Spain)

Three dimensional integrated circuits composed of vertically stacked active layer circuits allow shorter interconnections and hence leads to great possibilities to overcome the limits of 2D integrated circuits for carrying ICs further along the path of Moore's Law. Although the concept of 3D integration was originally reported in 1980's, only in recent years, the development of 3D tiered architectures enabled the creation of vertical interconnects. The greatest economic advantage of a 3D tiered architecture is greater yield. It is well-known that smaller chips have a higher yield, or alternatively, a lower defect rate when fabricated. Consequently, a higher yield can be achieved by partitioning a circuit into k smaller sub-circuits, each of which will be fabricated and stacked, than building a single larger chip that contains all of the sub-circuits on the same die.

Forthcoming electronics systems require the integration of new functionalities in one overall chip, defining the new design paradigm adopted in the EDA community known as System-on-Chip (SoC). As a result, I/Os are increasing in volume while chip size is decreasing, and new functions are integrated (passives, MEMS, optoelectronics, RF, etc). As consequence, the conceptual trend is to move from 2D configurations to 3D stacking and then to 3D-ICs to reduce package size, footprint, increase Silicon efficiency and have much short interconnects. More precisely, the key potential benefits of three 3D-ICs that can be identified are the following ones: power reduction, noise and jitter reduction, logical fan-out increase, performance improvement, functionality enhancement and density increase.

As a matter of fact, many different 3D construction methods have been proposed, but none of them has reached the maturity level to achieve its use in forthcoming nanometer scale electronics. In order to allow this novel integration technology to become a real alternative for the semiconductor industry, several key challenges need to be addressed, which spans from different manufacturing aspects to design automation. Thus, a very important collaborative work is needed in the near future between the manufacturing community for a reliable physical implementation and models, Electronic Design Automation society for CAD algorithms and tools, and finally verification community to provide effective testing mechanisms to validate the produced 3D chips for processing and communication architectures of electronic circuits.

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Upcoming Conferences*/Bill Joyner, william.joyner@src.org*	
PATMOS	Lisbon (Portugal), Sept. 10-12, 2008
Nano-Net	Boston (USA), Sept. 15-17, 2008
VLSI-SOC	Rhodes (Greece), Oct. 13-15, 2008
ESWEEK	Atlanta (USA), Oct. 19-24, 2008
ICCAD	San Jose (USA), Nov. 10-13, 2008
FMCAD	Portland (USA), November, 2008

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