JANUARY 2006

Currents

WELCOME TO THE INAUGURAL NEWSLETTER OF THE IEEE COUNCIL ON ELECTRONIC DESIGN AUTOMATION! We take this opportunity to introduce the mission and goals of IEEE CEDA. Why CEDA? Certainly, Design Automation as a subject area has been spread across a number of technical activities within IEEE, from monolithic circuits to large information processing systems. Within the context of electronic systems, when Computer-aided design (CAD) started as a discipline in the sixties it was synonymous with circuit simulation. Now, of course, CAD deals with a much broader set of concerns that continue to evolve with the technological advances in materials, processing, devices, circuits and systems, generally put under the umbrella of electronic design automation. On one side of the spectrum, the physical design of electronic circuits requires a deep knowledge of solid state circuits and more broadly electronic devices and interaction with specialists. On the other side, the ubiquitous presence of programmable processor cores in integrated circuits has shifted much CAD work into the design of embedded software and hardware/software co-design, areas traditionally covered by computer scientists. Indeed, combining theory and practice, CAD is a key technology that boasts its own thriving industry as well as an enabler for the much larger electronics systems industry.

So it was natural for such an activity to have a diversified footprint within the IEEE as a technical organization. While this diversity of CAD activities within the IEEE enabled the larger EDA community to benefit from significant cross-fertilization of ideas, as an organized activity, it made it much harder for the IEEE to serve the community with necessary and timely information and publications reflecting advances in the EDA area. Significant EDA related forums – conferences such as DAC and ICCAD, and publications such as IEEE Trans. On CAD, IEEE D&T – though highly regarded, were often deemed as secondary activities within the respective societies. This made it hard for the recognition of volunteer achievements, and execution of initiatives that demanded participation across different parts of the IEEE organization.

To ensure IEEE responsiveness to a technical community of over 5000 active members, a working group of EDA industry and academic leaders gathered in early 2004 to build a focal point that would be instrumental in supporting a vision of growth and renewal within the Institute and its Technical Activities Board. Working with a broad set of partners, the working group polled and conferred with all interested societies and councils within the IEEE to build the consensus for an organization that was officially approved first as an *ad hoc* committee in June 2004, and finally ratified as a council effective January 2006. Within IEEE Technical Activities, a council represents an organization with member societies. IEEE CEDA has six member societies, namely: Antennas and Propagation, Circuits and Systems, Computer, Electron Devices, Microwave Theory and Techniques, and Solid-State Circuits. As with any technical activity of the Institute, the ultimate goal is to advance the profession through a variety of technical activities from conferences, publications to standards. To serve its members spread across various member societies, the *Council* brings together several important resources, its community of contributors to sponsored conferences and publications. As of this writing, co-sponsored conferences include the Design Automation Conference (DAC), International Conference on Computer Aided Design (ICCAD) and Design and Test in Europe (DATE). In addition, CEDA also co-publishes IEEE Transactions on CAD and IEEE Design and Test of Computers. IEEE CEDA enjoys special relationships with focused technical activities such as the councils DATC, TTTC and the CANDE group.

With founding societies as members of the council, what does it mean for an individual to be a member of CEDA? The *Council* does not have official "members" as members are understood by the IEEE to be associated with dues (paid to the societies). Instead, individuals can

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sign up as "friends" of IEEE CEDA. Besides being 'friendlier', it also helps the emerging council move forward in building the community initiatives without being bogged down by issues associated with membership dues and its division across IEEE entities. The key to success of this formulation is the enormous support IEEE CEDA has received from its sponsoring societies.

The inaugural kickoff of IEEE CEDA was held at ICCAD in November 2005. The meeting included presentations and endorsements from the founding societies within the IEEE, the Special Interest Group on Design Automation (SIGDA) of the ACM and the Electronic Design Automation Consortium (EDAC). We are pleased to receive such a broad support and community momentum towards building the *Council*. We are also humbled by the challenges facing the community to continue to build on the pace of innovation in semiconductors by rapidly drawing new talent and entrepreneurship to the field, to engender technical activities that excite and challenge our audience and readership to new capabilities and opportunities. The diversity of the contributor backgrounds also demands council processes that encourage consensus building. In the very first few months, the *Council* converged on areas of technical interest and its constitutions and bylaws that were unanimously adopted by the founding members. The *Council* has now initiated a number of technical activities including sponsorship of the First IEEE Programming Challenge to be held at the International Workshop on Logic Synthesis, as well as participation in the DARPA/MTO activities in building the roadmap for electronic systems; both of these are described briefly in this newsletter.

This is a promising start of what we hope would be exciting years of innovation and invention in electronic design automation! These activities are made possible only through participation of our constituent membership. So get involved! If you have an idea or a suggestion, or are looking for a challenge in organizing a technical activity, workshop or a symposium, publication or a standard, please look us up on the web at **www.ieee-ceda.org**, contact any of the volunteer leads in respective areas, and, of course, remember to sign-on as a friend of IEEE CEDA!!

CEDA Sponsors First IEEE Programming Contest

Contributed by Stephen Edwards, Columbia University, sedwards@cs.columbia.edu

The *Council* will sponsor a programming challenge for the first time in the history of the **International Workshop for Logic Synthesis (IWLS)** to be held **June 7-9, 2006 near Denver, CO**. The goal is to build and foster a new open source logic synthesis system which will provide the base for future comprehensive EDA tool flows. Our long term goal is to build a complete RTL-to-layout implementation flow that also includes physical synthesis and optimization steps. Individuals as well as teams of students are encouraged to participate in this challenge to either implement their current research on this platform or to implement known and published synthesis algorithms as part of their education. For students who want to participate but lack concrete ideas, we will soon publish a list with suggestions of algorithms to implement.

The challenge is to implement one or more logic optimization algorithms on the industrial EDA database *OpenAccess*. The algorithms should make maximum use of the OpenAccess data base, be implemented in a native manner and adhere to the coding conventions of OpenAccess. The algorithm should be implemented within the **OA Gear** infrastructure described on the competition website. OA Gear provides an RTL-Verilog reader and synthesis into a technology independent netlist (and-inverter graph), a simple mapper which directly maps the nodes of the and-inverter graph onto a specified set of three library elements (AND, NOT, FF), accurate timing analysis with slew propagation, and a simple equivalence checker which is based on the and-inverter graph representation. The technology dependent optimization algorithms should be implemented directly on OpenAccess and should use the functional layer in OA Gear, in the package Func, together with the and-inverter graph (AIG) package. The results of the technology dependent algorithms are to be evaluated by performing accurate timing analysis and preferably use incremental timing analysis of the OA Gear timer.

The prizes include a travel grants as well as a cash prize of $500. Only full-time students registered during the spring 2006 semester are eligible to participate. The winners will be invited to either give a talk or present a poster as part of the workshop program. The submission deadline for the 2-page technical paper is **April 15, 2006**, and the deadline for the source code is **May 1, 2006** (midnight PST). For more information visit the website at **www.iwls.org/challenge**/.

CEDA Participates in DARPA Electronics Symposium, San Francisco, January 2006

The Charter of the Microsystems Technology Office (MTO) at DARPA is "to exploit breakthroughs in materials, devices, circuits and mathematics to develop beyond leading edge components with revolutionary performance and functionality to enable new platform capability for the Department of Defense." Practically, the MTO is tasked with programs related to integrated electronics and its ecosystem including photonics, MEMS and the EDA. MTO programs constitute a good fraction of the approximate $0.5B in material and electronics R&D (split evenly) that DARPA spends annually. These include a number programs of direct interest to CEDA community such as 3D Integrated Circuits, Chip-to-Chip Optical Interconnects, Clockless Logic, Distributed Macroelectronics, as well as the Focus Center Research Program that supports initiatives such as GSRC at Berkeley,

C2S2 at CMU, Interconnect Center at Georgia Tech, Material & Devices Center at MIT and Nano materials Center at UCLA.

The symposium, with attendance by invitation only, was an opportunity to look into the technical ideas and concepts that will lead to future high-impact MTO initiatives in integrated electronics. Majority of the presentations and discussions are related to new ideas and innovations that have not been published anywhere. DARPA is relatively a flat organization with front-line program managers who report to the Office Director who reports to the DARPA Director. The PMs are the primary interface to the technical community, as they seek out innovative ideas and accordingly formulate new DARPA initiatives. The MTO program managers who predominantly interface with EDA related activities (though not exclusively) are **Robert Reuss** and **Daniel Radack**. Both of them have graciously made themselves available to receive or discuss any ideas the EDA community members would have to address the mounting challenges in design, verification and test.

The Electronics Symposium was an intensive three-day affair with unclassified sessions ranging from nanotechnology, non-conventional electronics, non-silicon electronics, heterogeneous integration, to silicon platforms, design and design automation challenges. In his opening remarks, **John Zolper**, Director of MTO, outlined the MTO vision of enabling systems with evolving capabilities that requires a shift from static component performance to a new generation focused on reconfigurable systems, adaptive, and eventually intelligent components. While the reconfigurable systems and components consist of predefined deterministic set of operating parameters, the adaptable and intelligent systems are characterized by an increasing level of autonomy with the ability to reason and learn with time. Underlying these capabilities are advances in sensing, processing, actuation and power that are driven by advances in microelectronics. Examples of reconfigurable microsystems are in intelligent RF front-ends, microwave digital synthesizers, digitally controlled phase, amplitude and frequency modulation schemes and tunable pixels. The eventual goal is to build a new class of autonomous systems that sport human like sensor depth, capabilities to ensure persistent engagements and explore the extreme limits of power and volume. The current programs focus on extending performance through conventional and non-conventional means, by pursuing innovations in progression from new materials to new devices to new circuits and systems. These novelties are sought to overcome challenges related to scaling and density in microelectronics. These include: dealing with high defect rates, alternatives to lithography based manufacturing, interfaces to hybrid technologies and use of EDA and reconfigurability to offset mounting design challenges due to new materials, devices or even circuits types.

The participants discussed a number of emerging concepts and speculated on how various technologies may evolve. The important concepts relevant to our domain included use of *solution processing* that seek to build low cost flexible circuits through direct digital printing technology using nanoparticles. End of scaling (EOS) in CMOS devices and circuits occupied a significant portion of the discussions. The presentations included discussions on EOS impacts on physical design (regularized designs without use of SRAF structures, canonical shapes, sublithography patterning using self-assembly), electrical scaling (subthreshold electronics) and novel circuit structures including digitally dominated analog circuits. The takeaway messages were: while device level scaling knobs (such as gate length, gate oxide, mobility) may be maxed out, there exist several unexploited opportunities in scaling (e.g., through sublithographic patterning) that can continue to yield the scaling benefits. In the space between near-term device novelties such as FinFET, transport enhanced devices and 3D integration versus far-end nanoelectronics there is a significant space of new interface materials and device engineering that can enable a new generation of subthreshold electronics, with the capability to reach energy dissipation per function to theoretical limits which are about a 1000x less than current generation, operating at voltages in tens of millivolts. Longer term outlook focused on transition to well engineered novel devices that could be part of all silicon platforms containing electronics, photonics and sensors.

DARPA/MTO continues to drive innovations in miniaturization, function, power efficiency, system-on-chip and newer circuits fabrics. Many of these material and component advances are targeted for eventual advances in systems capabilities for adaptability and intelligence. There is a deep appreciation for the fact that such systems advances absolutely need advances in models, methods and tools to conceptualize, implement and validate such systems. EDA is thus a critical ingredient to the task. We welcome your participation in building the vision for DARPA-led technical initiatives in the area. Please contact **Louis Scheffer**, *lou@cadence.com* or **Rajesh Gupta**, *rgupta@ucsd.edu* for more information.

CEDA Distinguished Speaker Series

Contributed by Andreas Kuehlmann and Chuck Shaw, {kuehl, shaw}@cadence.com

The *Council* is initiating a Distinguished Speaker Series. Each event will feature the winners of the Best Paper Awards of at our premier forums (DAC, ICCAD, and IEEE Transactions on CAD). The authors of these papers will be invited to give an in-depth presentation of their work, going beyond the published paper and conference talk. Each talk will take place before a live audience of experts, and discussions will follow the presentation. The events will be video taped and posted on a CEDA web site.

The first event will take place this Spring in Silicon Valley. **Zhenhai Zhu** will discuss his William J. McCalla ICCAD 2005 Best Paper titled *Fast Stochastic Integral Equation Solver*. The second event will take place in July at DAC in San Francisco, in a session highlighting the first year's activities of CEDA.

CANDE Workshop to be held in Whistler, B.C., Canada in September, 2006

CANDE, the acronym for Computer-Aided Network DEsign, from the days when a "network" was another word for a "circuit," is the oldest continuing workshop in EDA since 1972. CANDE is a technical committee of the IEEE Circuits and Systems Society and IEEE CEDA. CANDE cosponsors the Design Automation Conference (DAC) and the International Conference on Computer Aided Design (ICCAD). This year's annual CANDE workshop will be held in **Whistler, B.C., September 21-23**. Key items on the agenda include:

- New cycles that could destroy the EDA industry
- The Shift of EDA Toward the "Edges"
- The Next Open Wave -- Open Hardware?
- Patent Process Opening and How it Affects EDA
- 5 Distruptive Technologies in the Next 5 Years

To participate, visit **www.cande.net** or contact the CANDE Publicity Chair, Sylvia Chanak, *syl@cadence.com*.

Upcoming CEDA Events/*Dick Smith, dsmith@topher.net*	
CODES+ISSS	www.esweek.org
DAC	www.dac.com
DATE	www.date-conference.com
FMCAD	www.fmcad.org
ICCAD	www.iccad.com
MEMOCODE	memocode.irisa.fr
MPSoC	tima.imag.fr/mpsoc
PATMOS	www.patmos-conf.org
VLSI-SOC	tima.imag.fr/conferences/VLSI-SoC06
Nano-Net	www.nanonets.org

Publications: Obsolete or Broken?

Contributed by Rajesh Gupta, VP, Publications

Internet search and rise of forums such as Google Scholar that provide access to both proprietary as well as freely available versions of research content are beginning to have a transformative influence on publications both as a scholarly activity as well as a business. Publications are intimately tied to the peer review process. While this process has always had its glaring examples of failures, from incompetent reviews to downright reviewer or editorial sabotage of the scientific progress, recent events such as discrediting of the stem cell work by Woo-Suk Hwang have called into question the ability of the peer review process to be a meaningful discriminator of the scientific progress and technological innovation. At its core, the peer review process represents a significant commitment to community service that is increasingly stressed by the growth in publication activity per researcher. When contrasted against the increasing democratization of the public media and the evolution of Web from a publishing medium to an interactive, two-way collaboration medium, the fundamental assumptions underlying the publications activity including expert approval, control of the publication venues by the selected and even associated financial models driving publications have come under stress. Anonymous and blind reviews are increasingly hard to conduct and perhaps more importantly these are increasingly irrelevant. Perhaps, we need modalities where opinions and reviews of a paper are as much a part of the technical content as the submission itself. This would make the review process more accountable and more rewarding to the conscientious reviewers who must toil in anonymity only to see poor content appear in alternative forums anyways. Or as an alternative, perhaps content evaluation should move to be primarily a post-publication activity with editorial discrimination (and its co-published justification) replacing the review-driven selection from submitted content?

On the financial front, electronic dissemination through library packages represents a significant fraction of income for many IEEE publications. The revenue sharing formulae from aggregated packages such as *IEEE Xplore* reward short articles that capture the latest trends with the highest number of clicks rather than labored lengthy papers that take much longer time to produce, review and publish. No wonder that many publications including our own transactions are seriously considering placing limits on the size of the articles, partly in an effort to improve reviewer response and partly to maximize technical richness and diversity within allocated page budgets.

While changing technological realities have an impact on our publications, their lasting effects can not always be anticipated or predicted. Against this backdrop, we welcome your ideas and opinions on how we can ensure that our publications are meaningful and useful to our readership.