



## IEEE Council on Electronic Design Automation

### *The Silicon Integration Initiative: Driving Industry Collaboration*

*By Steve Schulz, President & CEO*

Open standards provide the structure for the interdependent network of hundreds of companies to work together within the design eco-system, supporting critical innovation through collaboration. The Silicon Integration Initiative (Si2) has been facilitating this collaboration with the semiconductor and EDA industries for 20 years. Some of the features of Si2 that contributed to this fact are the following

#### **Holistic, Market-Centric Approach**

Si2's mission, to improve interoperability and integration across IC design flows, is centered on successful market adoption. This goal drives everything we do at Si2, from careful selection of proposed projects, to a holistic market-enabling perspective that includes collaborative software, on-line training, technical workshops, web infrastructure, marketing, legal - and an emphasis on complete flows, not just file formats. Every project under Si2 has active program management and engineering support with full-time staff.

#### **End-User Requirements, Supplier-Centric Solutions**

Si2 was established by leading semiconductor companies that shared a vision for industry. Now, over 70 EDA companies have joined, along with fables, foundry, and IP members. Still, all Si2 coalitions are chaired by end-users to ensure the resulting standards have real market traction. Seven of Si2's ten elected Board of Directors seats are designated for end-user companies, two for suppliers, and one reserved for smaller companies.

#### **Dedicated Engineering Expertise**

Si2 provides active program management for every coalition and working group, offloading administrative logistics so that domain experts can focus on deliverables. Si2 engineering includes experienced industry veterans with semiconductor expertise spanning from process design kits (PDKs) and transistor level circuit design, through

physical design, up to logical and even system-level design. Software expertise spans all major programming and scripting languages, relational database technology, software architecture design, and application programming interfaces. Si2 engineering services include in-house development of standards specifications and technical reference guides, technical training classes and labs, custom web-site design and development, and full-time IT support for all dedicated servers and web applications.

#### **Intellectual Property And Licensing Trends**

Both semiconductor design and EDA tools continue to increase in complexity, demanding standards of increased sophistication - and by consequence involving more IP of greater value. Recent standards-related lawsuits have heightened awareness of the risks of using, or contributing, valued IP in the course of standards development.

Si2 members have always had unique protection from "treble damages" in anti-trust lawsuits, by virtue of our federal charter. Si2 has brought together lawyers from member companies to craft a new IP policy representing the best current practices. All recent coalitions utilize this policy, helping to assure members that today's investment in developing standards will not hit adoption barriers - or threaten their own IP portfolios.

#### **Open Evolution: Open Source Model for Standards**

When companies join together to define a new standard, they do not expect that standard (or related software) to splinter in costly and confusing directions, diluting its value and creating inefficiencies for the industry. Unfortunately, this has occurred repeatedly within EDA. Si2 explicitly prevents splintering of Si2 standards through an open community licensing model we call "Open Evolution". Rooted in the open source model, it ensures that any company has equal opportunity to join the community determining the standard's direction. This model guarantees that each new version cannot be forked due to near-sighted competitive forces. This feature also extends to software reference implementations, parsers, and some supporting utilities.

*Steven E. Schulz* [steve@si2.org](mailto:steve@si2.org)

## ***Call for Proposals of services needed to Younger EDA Professionals***

A recent collaborative initiative of IEEE is trying to address the problem of how to help students and young engineering professionals on the subject of career activities. Specifically, this collaborative initiative has selected a set of GOLD members, who are important young professionals already involved in the different Technical Societies and Organizational Bodies of IEEE, as well as Technical Activities volunteers, to pursue the idea of establishing a single web portal allowing students or young professionals to access Young Career support areas. These areas already appear in the websites of the Societies and Councils.

In this regard, Prof. David Atienza (EPFL) is a GOLD member serving on the CEDA Executive Committee, and has been selected as CEDA GOLD Coordinator. Therefore, he is in charge of helping CEDA and IEEE to identify activities that can help the younger EDA professionals. Furthermore, he is definitely interested in receiving any proposal about additional services that would be of use to younger EDA professionals.

David Atienza [david.atienza@epfl.ch](mailto:david.atienza@epfl.ch)

## ***Hardware/Software Co-Design Contest***

The third annual HW/SW Co-Design Contest will be held in conjunction with the Seventh ACM-IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE'2009). The challenge is to build a working hw-sw co-design solution, given a 1-month design challenge, using all co-design tricks of the trade. A design on paper is not enough to win. You must build a working demonstrator on an FPGA platform.

The design challenge will be posted on March 1, 2009, 12:01AM ET, closing on March 30, 2009, 11:59PM. There are multiple cash prizes for winning teams, and top winners will be invited to present their designs and publish short papers at MEMOCODE-09 (Cambridge, MA, July 13-15). A team may include both industry and academic members with no limit on the size of a team or the number of teams per institution. Each person can participate in only one team. The hardware/software co-design contest is organized by James C. Hoe (CMU) and Forrest Brewer (UCSB).

For further information, please visit [www.memocode-conference.com](http://www.memocode-conference.com)

## ***Preview of MSE 2009***

Reported by Andrzej Rucinski (UNH)

The IEEE Computer Society International Conference on Microelectronic Systems Education is the premier

conference dedicated to furthering undergraduate and graduate education in designing and building innovative microelectronics systems. The conference is held in the U.S. in odd years, and in Europe in even years, when it is called the European Workshop on Microelectronics Education (EWME). MSE is co-located with the Design Automation Conference (DAC).

The MSE conference provides an excellent opportunity for educators and industry to work together to ensure continued excellence in the field of microelectronic systems. Of particular interest is incorporation of trends in the microelectronic system industry and research into the classroom. This year's theme, "Educating System Designers in the Multi-core, Ubiquitous Computing Era," brings together current relevant topics including omnipresent electronics in the form of cell phones, mp3 players, and even wearable computers.

Papers will include the following areas: education techniques, industry and academic collaborative programs, educational infrastructure, novel education strategies for embedded processors, VLSI design, CAD, FPGAs, etc.

For further information, please visit [www.mseconference.org](http://www.mseconference.org)

## ***Roychowdhury, Philips elected IEEE Fellow for 2009***

IEEE recently announced the 2009 class of IEEE Fellows. The list included Jaijeet Roychowdhury and Joel Philips with IEEE CEDA serving as the nominating organization. Jaijeet Roychowdhury (UC Berkeley) was recognized for his "contributions to simulation and automated macromodelling of integrated circuits". Joel Philips (Cadence Research Labs) was honored for his "contributions to numerical techniques in the design of high-frequency and radio frequency systems". IEEE Fellow is the highest honor for IEEE members. The grade of Fellow recognizes unusual distinction in the profession and the IEEE looks to the Fellows for guidance and leadership. As an organized unit of IEEE, IEEE CEDA is happy to help with the identification, nomination and evaluation of candidates in its field of interest. Selection of fellows is done through a process conducted by the IEEE board of directors. The deadline for nominations for 2010 fellows is March 1, 2009. Further information at [http://www.ieee.org/web/membership/fellows/Fellows\\_Class\\_of\\_2009.html](http://www.ieee.org/web/membership/fellows/Fellows_Class_of_2009.html)

| Upcoming Conferences / Bill Joyner, <a href="mailto:william.joyner@sra.org">william.joyner@sra.org</a> |                                       |
|--------------------------------------------------------------------------------------------------------|---------------------------------------|
| DATE                                                                                                   | Nice (France), April 20-24, 2009      |
| GLSVLSI                                                                                                | Massachusetts (USA), May 10-12, 2009  |
| MEMOCODE                                                                                               | Cambridge (USA), July 13-15, 2009     |
| DAC                                                                                                    | San Francisco (USA), July 26-31, 2009 |

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