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CEDA Currents

IEEE Council on Electronic Design Automation

TCAD Best Paper Award

I recently had the pleasure of a ringside view of the selection process for the annual Donald O. Pederson *TCAD* (*IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*) Best Paper Award. Any paper that has appeared in *TCAD* over the past two calendar years is eligible for this award. The winner of this year's award was "FLUTE: Fast Lookup Table Based Rectilinear Steiner Minimal Tree Algorithm for VLSI Design," by Chris Chu and Yiu-Chung Wong (*IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 27, no. 1, 2008, pp. 70-83)—an impressive work on fast routing algorithms.

This research addresses a fundamental problem in computer science: building Steiner minimum trees. This topic has applications in diverse fields such as IC design, networking and communications, traffic engineering, brain networking, and phylogenetic trees in bioinformatics. The problem is easy to state, but hard to solve optimally: given a set of points in space, find the best structure that connects these points.

As we map this statement to the routing problem in chip design, an additional restriction is imposed: the wires must run parallel or perpendicular to one another (that is, on a Manhattan grid), and the goal is to minimize the wire length for the route. This problem is known to be NP complete (ergo difficult) and is certainly not new; several talented researchers have banged their heads against it over the decades.

The novelty of this paper is in developing a computationally efficient algorithm with a clever acronym—Flute (fast lookup table estimation). The core idea of the approach is to classify nets in terms of their pin locations, and to group nets into equivalence classes that have similar properties. The key properties of these equivalence classes are precharacterized and stored in a lookup table. For any routing problem, the appropriate equivalence class is identified, and the entries in the lookup table point to a fast evaluation of the optimal Steiner tree.

However, the size of this lookup table grows rapidly (factorially) with the number of pins. So, this method is practical only for trees with a small number of pins. Fortunately, practical designs contain many nets with nine or fewer pins, for which the problem is tractable. Larger nets are split into smaller subnets, and the lookup table approach is then applied to individual subnets—at some loss in optimality, but with a massive gain in runtime and storage overheads.

This work has had excellent practical impact, and academic researchers and industry practitioners have widely adopted Flute-based methods, making this work an excellent exemplar of how theoretical techniques can be brought to bear upon intensely practical problems. In other words, it is a great choice for the Pederson award!

How was the *TCAD* Best Paper selected? In accordance with past practice, the procedure involved a detailed nomination and voting process. In the first round, about 20 papers were nominated for consideration, spanning all areas of CAD. Next, the *TCAD* editorial board was polled, and members were asked to provide their top two choices for the award. These choices were used to generate a short list. Then, in the final round of voting, the Best Paper was selected. Several outstanding papers were in contention for the award. However, throughout the voting process, the Flute paper was consistently ahead in the competition, and was a resounding winner in the final round of voting.

So, that's the story of this year's Best Paper Award.

One last note: at *TCAD*, we welcome your input at all times. If you have ideas to improve our processes, or to make our journal more relevant, or if you want to suggest special-section topics or anything else, please don't hesitate to get in touch with us.

Sachin S. Sapatnekar (EIC of TCAD*)*

CTO Steve Teig Discusses Approach for Beyond von Neumann Computing

Steve Teig, president and chief technology officer (CTO) of Tabula will describe an approach to move beyond von Neumann computing during a luncheon hosted by the IEEE Council on Electronic Design Automation at this year's Design Automation Conference (DAC) on Tues-

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day, 15 June 2010 (from noon to 2 p.m. in Room 303 of the Anaheim Convention Center in Anaheim, California). The lunch is open to all DAC attendees on a first-come, first-served basis.

Inventor of Tabula's Spacetime 3-Dimensional Programmable Logic Architecture, Teig will describe a simultaneous approach to the design of architecture, hardware, and software. He sees these as aspects of a cohesive whole, similar to the way John von Neumann (inventor of the von Neumann architecture) and Alan Turing (developer of the Turing machine) did. Teig believes that a new approach to architectural design will maximize the opportunities to go beyond von Neumann computing.

Prior to cofounding Tabula, a fabless semiconductor company that has developed a new category of 3D programmable logic devices (3PLDs), Teig was co-CTO of Cadence Design Systems. He had joined Cadence through its acquisition of Simplex Solutions, where he had been CTO. He has cofounded two successful biotechnology companies, CombiChem and BioCAD, as well as an EDA company, Tangent Systems. He holds more than 220 patents.

Shishpal Rawat, shishpal.s.rawat@intel.com

DAC "Birds of a Feather" Discussion on Trends in Social Media

CEDA will host a "Birds of a Feather" session during DAC on social media, moderated by Shishpal Rawat, vice president of technical activities for CEDA and director at Intel of Business Enabling Programs and EDA Investments. This discussion will be held on Tuesday, 15 June 2010 (from 6:30 pm to 8:00 p.m. in Room 209 of the Anaheim Convention Center).

The discussion will focus on trends in social media and ways to better use social-media channels to reach a wider EDA audience. This session will attempt to determine which mechanisms the EDA community uses and how best to utilize them.

For more details, visit the CEDA: www.c-eda.org

Papers in IEEE Embedded Systems Letters

The top-five accessed articles from *IEEE Embedded Systems Letters* during April 2010 were as follows:

- "An FPGA-Based Framework for Technology-Aware Prototyping of Multicore Embedded Architectures," by P. Meloni et al.
- "An Analyzable Memory Controller for Hard Real-Time CMPs," by M. Paolleri et al.
- "Efficient Software Synthesis for Dynamic Single Appearance Scheduling of Synchronous Dataflow," by W. Liu et al.
- "Hardware Resource Virtualization for Dynamically Partially Reconfigurable Systems," by H. Chun-Hsian et al.
- "Evaluation of Dynamic Profiling Methodologies for Optimization of Sensor Networks," by A. Shenoy et al.

Upcoming Conferences (Bill Joyner, william.joyner@src.org)	
MEMOCODE	Grenoble, France, 26-28 July 2010
FMCAD	Lugano, Switzerland, 20-23 Oct. 2010
ICCAD	San Jose, California, 7-11 Nov. 2010

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