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Currents

IEEE Council on Electronic Design Automation

CEDA Launches IEEE D&T Electronic Edition

Working in cooperation with IEEE Computer Society Press, the *Council* is pleased to announce the availability of **IEEE D&T Electronic Edition**. The electronic edition is specially designed by QMAGS publishers to be delivered to CEDA affiliates via the internet. The Electronic Edition is exact cover-to-cover copy of the printed magazine, including all illustrations, graphics and conference calls and other advertising in a QuVu format that fits the computer screen perfectly and does not require page manipulations. This compact and highly navigable form is delivered to you every two months for a subscription price of $19.95. This is half the price of the best member rate for subscription to regular D&T print issue. Even more importantly, signing through CEDA, you do not need to be a member of IEEE or any society to receive the best rates. For more information and to sign-on please visit *Council* website at www.ieee-ceda.org.

CEDA Sponsors IC Routing Contest at ISPD

The *Council* co-sponsored the International Symposium on Physical Design (ISPD) with ACM on March 18-21, 2007. An IC global routing contest, sponsored by the *Council* and SRC, was held at the symposium to showcase new directions for research in IC routing algorithms. Two sets of benchmarks were released, corresponding to 2D and 3D routing instances. Teams were invited to produce global routing solutions for the benchmarks. Prizes were awarded for the entry that achieved the best overall results in each category. In addition, the *Council* sponsored a prize for the best results achieved by an openly available router.

Eleven teams from academic and research institutes participated in the ISPD contest. "The purpose of the contest is to guide researchers toward most urgent challenges in the EDA industry, and also to map out state-of-the-art solutions," said ISPD 2007 chair Patrick Madden, professor at the State University of New York.

Routers were compared based on the number of routing violations (overflows) and total routing wire length. David Pan, ISPD 2007 program chair and professor at the University of Texas at Austin, noted that there is still some controversy over the methods used to compare routers. "The ISPD community is still trying to define a good metric," Pan said. The winning entry in the 2D category was "*Fairly Good Router* (FGR)," written by Jarrod Roy, a graduate student at the University of Michigan. "We plan to open-source it to boost research in routing and help improve commercial EDA tools," said Igor Markov, professor at the University of Michigan. The winner of the 3D category was *MaizeRoute*, written by Michael Moffitt, also a graduate student at the University of Michigan.

"High-quality and publicly available global routers will be very helpful for CAD research," said Lou Scheffer, Cadence Design Systems fellow and ISPD 2006 chair. "Also, existing global routers should make it easier to build an academic detailed router — perhaps our contest for next year."

MEMOCODE 2007 Co-Design Contest

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New to the *Council* co-sponsored IEEE/ACM MEMOCODE 2007 Conference is the HW/SW Co-Design Contest. The goal of the co-design contest was to identify issues specific to the co-design practice and to foster greater interest in the design aspects of the MEMOCODE conference. The contest would also serve to showcase advances in co-design tools and methodologies. To make a contest feasible, we decided to keep the

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term relatively short and to provide a working code base for at least one inexpensive and easily available platform. We ultimately opted for a problem that we gauged could be done well in a week and allowed the contestants a month lead-time to solve it.

We did not wish to limit the competition to a particular execution platform since we thought that many design groups would be more familiar with their preferred platforms. Instead, we left the choice of platform to the contestants and provided a grading metric that attempts to equalize the differences. We did, however, select the Xilinx XUP2VP prototyping board as the reference platform. The XUP2VP board provides a large variety of interfaces, is well supported, and is inexpensive. The on-board Virtex 2 FPGA (XC2VP30) has a substantial programmable logic fabric, a fair amount of on-chip memory, and two PowerPC 405 embedded processors. For the XUP2VP environment, we provided reference starter design materials, including a software-only reference solution and a reference HW/SW interface library comprising ready-to-use C functions and Verilog modules.

The design problem chosen was the Blocked Matrix-Matrix Multiplication. The basic algorithm, though fundamentally simple to understand, lends itself to a large space of high-leverage optimizations in managing data movement, storage, and bandwidth. We designed the problem to require hardware involvement in the design as well as a software component.

We focused on performance as the primary metric of merit. The metric used is the speedup achieved by the contestants' design relative to the official software-only reference design on their platform of choice. We further asked the contestants to describe the design in sufficient detail so that a panel of judges could make decisions about the 'elegance' of the approach as well as the efficacy of a particular design. We felt that it was important for the judging panel to be able to reward a unique or novel solution even if its overall performance is less competitive.

Two teams, from MIT and Virginia Tech respectively, successfully submitted a final design. Both teams were invited to present at the conference with conference provided travel support. Brief write-up of their solutions is also included in the formal conference proceedings. Although the contest did not have the number of entrants as we had hoped, the two finished entries are of very high quality and offer real technical contributions to share with the conference audience. We believe the co-design contest adds an important new dimension to the MEMOCODE conference and should remain a valuable component of the MEMOCODE conference in the future. The call-for-participation is available at the website http://memocode07.ece.cmu.edu/contest.html.

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Join us for CEDA Distinguished Speaker Event at DAC:
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