CEDA Currents
Council on Electronic Design Automation

T.W. Williams Wins EDAA Lifetime Achievement Award

The European Design and Automation Association has awarded the 2007 EDAA Lifetime Achievement Award to Thomas W. Williams for his outstanding contributions to the state of the art in testability of electronic circuits, and specifically to full-scan design. This award is given to candidates who have made innovative contributions that have impacted the way electronic systems are designed. Past recipients include Kurt Antreich (2003), Hugo De Man (2004), Jochen Jess (2005), and Robert Brayton (2006).

Thomas W. Williams is a Synopsys Fellow and an adjunct professor at the University of Calgary, Alberta, Canada. He has also served at IBM Microelectronics Division in Boulder, Colorado, as manager of the VLSI Design for Testability Group, which dealt with DFT of IBM products. Williams has a BS in electrical engineering from Clarkson University, an MA in pure mathematics from the State University of New York at Binghamton, and a PhD in electrical engineering from Colorado State University. Along with Edward B. Eichelberger, Williams published the first paper on the level-sensitive scan design (LSSD) technique for testing logic circuits. Since then, he has been leading, defining, and promoting DFT concepts and has significantly influenced the IC design community to adopt full scan as a de facto standard. As a result of his efforts, the EDA industry has been able to base many of its leading tools on the foundation of the full-scan design structure. Prior to the adoption of full scan, the industry had to deal with the sequential complexity of a nonscan design. Now, full-scan design has become a pragmatic basis for a range of today's design tools, including mainstream logic synthesis, static timing analysis, and formal-verification solutions.

Williams was also a founding member of the IEEE Test Technology Technical Committee. In 1978, he started the first TTTC workshop—the DFT workshop also known as the "Vail Workshop," which was the first test workshop of any kind. He also cofounded the first test workshop in Europe, the European DFT Workshop. This later grew into the European Test Conference and then into a significant portion of the Design, Automation and Test in Europe Conference (DATE).

He has authored several seminal papers related to test technology and scan design. An IEEE Fellow, Williams has received several awards, including the W. Wallace McDowell Award from the IEEE Computer Society (which he shared with Ed Eichelberger in 1989). In 1997, he was presented the IBM Corporation Award for Test.

For more information about this award, contact Bernard Courtois (bernard.courtois@imag.fr).

Richard Newton Passes Away

EDA pioneer A. Richard Newton, Dean of Engineering at the University of California, Berkeley, passed away on 2 January 2007. The news came as a shock to the entire community. In a short span, Richard Newton wore many hats and contributed to the society in so many ways as an academic, an entrepreneur, an administrator, but above all as a visionary with enormous compassion. He made seminal research contributions to the EDA field and helped found key EDA companies, including SDA Systems (now Cadence Design Systems), Crossbow, and Synopsys. From 1998 to 2002, he was a venture partner with Mayfield Fund, a respected Silicon Valley VC firm.

Both our flagship publications will carry formal obituaries: In the Jan-Feb 2007 issue of *IEEE Design and Test*, Aart De Geus from Synopsys gives a personal account of Newton's life and contributions to the EDA industry; and, later in the year, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* will publish a recollection from Newton's colleagues in academia. For more information about the life and accomplishments of Richard Newton, please visit http://www.coe.berkeley.edu/newsroom/newton.

Second IEEE Programming Challenge at IWLS

CEDA is sponsoring the second IEEE Programming Challenge at the 16th International Workshop on Logic & Synthesis (IWLS 07), to be held 30 May-1 June, in San Diego, California. The last programming challenge was a great success, and the winning submissions are now

0740-7475/07/$25.00 © 2007 IEEE Copublished by the IEEE CS and the IEEE CASS

open source, released as part of the OpenAccess (OA) Gear infrastructure. With this programming challenge, the organizers would like to advance and promote an open-source logic synthesis system that provides the basis for future comprehensive EDA tool flows, and a research platform based on the OpenAccess database.

Individual students, as well as teams of multiple students, are encouraged to participate in this challenge to either implement their current research on this platform or implement known and published synthesis algorithms as part of their education. A list of suggested algorithms is available at http://www.iwls.org/challenge.

The Challenge

The challenge is to implement one or more logic optimization or verification algorithms on the OpenAccess industrial EDA database. The algorithms should make maximum use of the OpenAccess database, be implemented in a native manner, and adhere to the coding conventions of OpenAccess.

The algorithm should also be implemented within the OA Gear infrastructure. OA Gear provides an RTL Verilog reader and synthesis into a technology-independent netlist, an AIG (and-inverter graph); a simple mapper that directly maps the AIG's nodes onto a specified set of three library elements (AND, NOT, and FF); accurate timing analysis with slew propagation; and a simple equivalence checker based on the AIG representation.

Technology-dependent optimization algorithms should be implemented directly on OpenAccess. Technology-independent algorithms should use the functional layer in OA Gear, along with the AIG package. Participants should evaluate the results of the technology-dependent algorithms by performing accurate timing analysis, preferably the incremental timing analysis of the OA Gear timer.

The Prizes

The following prizes will be awarded to winning participants:

- For a fixed number of significant contributions—a travel grant for one team member to attend IWLS 2007, including airfare (up to a fixed cap), full registration, and lodging.
- For a single outstanding contribution—a cash prize of $500 (in addition to the travel grant to IWLS).

Only full-time, currently enrolled students are eligible to participate. The winners will be invited to either give a talk or present a poster as part of the IWLS program.

The Dates

- Submission deadline for preliminary version of two-page technical paper: 15 April 2007
- Submission deadline for final two-page technical paper: 24 April 2007
- Submission deadline for source code: 28 April 2007
- Notification of winners of travel grants: 9 May 2007
- IWLS workshop: 30 May-1 June 2007

For more information about the awards criteria, winning submissions of the previous programming challenge, or how to get started and download the software, go to http://www.iwls.org/challenge. For any further queries, contact iwls-challenge@spacedog.fishkill.ibm.com. This is an annual event.

Upcoming CEDA events

7th International Forum on Application-Specific Multi-Processor SoC (MPSoC)
25-29 June 2007
Hyogo, Japan
http://tima.imag.fr/mpsoc

International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS)
3-5 September 2007
Göteborg, Sweden
http://www.ce.chalmers.se/research/conference/patmos07

IEEE/ACM International Conference on Computer-Aided Design (ICCAD)
4-8 November 2007
San Jose, Calif.
http://www.iccad.com

CEDA Currents is a publication of the IEEE Council on Electronic Design Automation. Please send contributions to Kartikeya Mayaram (karti@eecs.oregonstate.edu) or Preeti Ranjan Panda (panda@cse.iitd.ac.in).