NOVEMBER 2007 Currents

CEDA

IEEE Council on Electronic Design Automation

CEDA Reappoints Enrico Macii as EIC and Sachin Sapatnekar as Deputy EIC of IEEE Transactions on CAD/CAS

Contributed by Rajesh K. Gupta, VP Publications

Council executive committee and board-of-governors have unanimously approved recommendation by CEDA Publications of reappointment of Enrico Macii as the Editor-In-Chief of IEEE Transactions on CAD/CASS (TCAD) for two years beginning January 2008. Sachin Sapatnekar will also continue in his role as Deputy EIC of TCAD during this period.

In the two-year period since their appointment in January 2006, the Macii/Sapatnekar team's achievements include:

a. reduction of publication backlog from 223 papers / 14-month delay to 106 papers and 6-month delay currently; reduction in the time to first decision from 90 days to 74 days currently;

b. reduction in acceptance ratio from 60% to 41.5% over the duration of his leadership. The acceptance ratio is steadily below 40% since 11/06 and seems to be heading for a more reasonable 35-40% over the long term;

c. transitioned and managed the TCAD electronic submission and review system and launched the TCAD monthly newsletters with links to papers in IEEE Xplore;

d. enhanced keywording and advance online availability of the papers accepted improving our all-important Xplore hits to recent TCAD articles;

As a consequence of this leadership, not only TCAD is serving its readership community with timely articles but also has enjoyed increases in its financial bottom line that has allowed the council to continue to invest into improving the responsiveness of TCAD to its authors. The *Council* will continue to augment TCAD page budgets by almost 500 pages in the coming two years. As always, it is our authors, readers and volunteers who are key to success of our publication efforts. If you are interested in volunteering for TCAD or other publications, feel free to contact the TCAD or publication leadership at enrico.macii@polito.it or rgupta@ucsd.edu.

IEEE Prohibited Authors List Updated in August 2007

IEEE takes ethical issues related to peer-review and publications seriously and has worked out a detailed process for handling complaints regarding plagiarism, multiple submissions or other ethical violations. As a consequence of this effort, IEEE periodically updates its Prohibited Authors List (PAL) that bars identified authors from consideration at any IEEE publications for specified periods. This list is available only to the leadership of IEEE publications. For more information on the process and contact information please visit IPR office at: http://www.ieee.org/copyright.

Robert Brayton To Be Honored as Kaufman Award Winner

Dr. Robert K. Brayton, Cadence Distinguished Professor of Electrical Engineering and Computer Science at the University of California at Berkeley, has been chosen as this year's recipient of the Phil Kaufman Award for Distinguished Contributions to Electronic Design Automation (EDA). The award, jointly sponsored by the IEEE Council on EDA and the EDA Consortium, will be presented to Dr. Brayton in a ceremony preceding ICCAD in November.

"IEEE places a high value on rewarding individuals such as Bob Brayton who have made contributions that significantly impacted the EDA community," remarks Al Dunlop, president of the IEEE Council on EDA. "Bob's technical contributions are at the basis of most of the offerings of our industry today."

Dr. Brayton's seminal contributions to logic synthesis have been critical to the design of application-specific integrated circuits (ASICs) and the development of CAD products that use logic synthesis software. Additionally, he co-developed the Sparse Tableau Approach and the

CEDA Currents is a publication of IEEE CEDA. Please send contributions to Kartikeya Mayaram, karti@eecs.oregonstate.edu, Preeti Ranjan Panda, panda@cse.iitd.ac.in or Anand Raghunathan, anand@nec-labs.com.

Backward Differentiation Formulas. Their implementation as early Circuit Simulation software influenced SPICE, HSPICE™ and Spectre®.

From 1961-1987, Dr. Brayton worked for the IBM Thomas J. Watson Research Center in Yorktown Heights, N.Y., where he and his colleagues worked on Yorktown Silicon Compiler that led to combining synthesis and place and route techniques.

A professor at the University of California at Berkeley since 1987, Dr. Brayton is an IEEE Fellow, a member of the National Academy of Engineering. He has received the IEEE Circuits and Systems Technical Achievement Award, the Circuits and Systems Golden Jubilee Award, the IEEE Millennium Medal and the Emanuel R. Piore Award. Dr. Brayton received the 2006 European Design Automation Society lifetime achievement award. He has published 10 books and more than 450 papers.

Dr. Brayton earned a bachelor of science degree in Electrical Engineering from Iowa State University in Ames, Iowa, and a Ph.D.in Mathematics from the Massachusetts Institute of Technology in Cambridge, Mass.

Presented annually since 1994, the Phil Kaufman Award honors an individual who has had a demonstrable impact on the field of EDA. It was established in honor of deceased EDA industry pioneer Phil Kaufman, who turned innovative technologies such as silicon compilation and emulation into businesses that have benefited electronic designers. Nominations for the 2008 Award are due Monday, June 30, 2008. For more information on the award, go to www.edac.org or ***www.ieee-ceda.org***.

CANDE Holds A Successful Workshop On Queen Mary

CANDE, the venerable group of EDA stalwarts, thought leaders and decision makers, held its annual workshop on Queen Mary in Long Beach, September 6-8, 2007. Program included sessions on Multi/Many Core Chips, Statistical Design, Nano/Bio Design and Keynote talks by Drew Endy, MIT on "Technologies for Engineering Biology" and by Bill Joyner of SRC on "CAD and the Queen Mary: Tied Up at the Dock?". As always, CANDE sessions were live though a few speakers did make it to their last slide. While CANDE does not publish official records or proceedings, you can find slides of the presentations at http://www.ece.utexas.edu/~dpan/CANDE2007Slides_AttendeesOnly. More information on CANDE is available on CANDE website at http://www.cande.net/

Gary Smith to receive ACM Award

Contributed by Gabe Moretti

SIGDA/ACM has recently announced that Gary Smith, founder and Chief Analyst for Gary Smith on EDA (GSEDA), has been selected as recipient of a 2007 Computing Machinery/Special Interest Group on Design Automation (ACM/SIGDA) Distinguished Service Awards in recognition for his contributions as Chief EDA Analyst at Gartner Dataquest for the past two decades. While at Gartner Dataquest, Mr. Smith led a team of recognized analysts and best known for their Gartner Dataquest Annual Report at the Design Automation Conference. Mr. Smith and his team have been instrumental in reporting on and identifying industry trends in Electronic System Level (ESL), Electronic Design Automation (EDA) and Embedded Systems industries. Earlier, Mr. Smith was a consultant in design methodology and worked in the ASIC end of the semiconductor business. While at LSI Logic, Mr. Smith became an evangelist for the RT-level design methodology. Starting in the semiconductor industry, Mr. Smith was involved in some of the first attempts at customer-designed ICs.

The award will be presented to Mr. Smith at the IEEE/ACM International Conference on Computing Aided-Design (ICCAD) during the opening session on the morning of Tuesday, November 6, 2007 at the DoubleTree Hotel, San Jose, CA.

MEMOCODE Colocated With DAC 2008

IEEE/ACM Conference on Models and Methods for Codesign (MEMOCODE) will be collocated as a sister conference to be held June 5-7, 2008 in Anaheim Convention Center, Anaheim, California. The conference features a design contest that seeks to demonstrate value of system-level design tools and methods on real-life designs in a competitive environment. For more information, visit conference website at http://www.memocode-conference.com/

Watch this space for Upcoming SRC/GRC and FCRP Funding Opportunities

The Global Research Collaboration (GRC) arm of the Semiconductor Research Corporation conducts mission-driven research on behalf of its members companies responding to broad industry needs in semiconductors. First step in this process are calls for white papers in response to identified industry needs in various areas grouped under thrusts related to "Computer Aided Design and Test", "Design Sciences", "Integrated Circuit and Systems", "Interconnect and Packaging", "Nanomanufacturing" and crosscutting/cross-disciplinary thrusts. While no calls are currently open, it is anticipated that Design Sciences and CADTS will open calls in October and December this year. For more information, please visit: http://grc.src.org/.

Focus Center Research Program (FCRP) is managed by the directors of five FCRP research centers in charge of research addressing long term industry needs. While no specific calls are active, please contact center directors directly. More information can be found at: http://www.src.org/member/about/funding.asp

Upcoming Conferences

Contact Dick Smith

CODES+ISSS part of Embedded Systems Week (ES Week), http://www.esweek.org/

September 30-Oct 5, 2007, Salzburgh, Austria

Nano-Net, International Conference on Nano-Networks, September 24-26, 2007, Catania, Italy. Http://www.nanonets.org/

VLSI-SOC

ICCAD, 2007 International Conference on Computer-Aided Design, November 5-7, 2007 DoubleTree Hotel, San Jose, California, http://www.iccad.com/

FMCAD, Formal Methods in CAD, November 11-14, 2007, Austin, TX. http://www.fmcad.org/

DATE, Design, Automation and Test in Europe, March 10-14, 2008, Munich, Germany

http://www.date-conference.com/

NOCS: International Symposium on Networks-on-Chip, April 7-11, 2008, Newcastle University, http://www.nocsymposium.org/

Most-Downloaded Articles in 2006

Article	Downloads
IEEE Design & Test of Computers	
"Embedded systems and the kitchen sink," vol. 23, no. 1, Jan.-Feb. 2006	452
"Dynamic Power Management in Wireless Sensor Networks," vol.18, no. 2, Mar.-Apr. 2005	423
"Physical design for 3D system on package," vol. 22, no. 6, Nov.-Dec. 2005	381
"Design, synthesis, and test of networks on chips,", vol. 22, no. 5, Sep.-Oct. 2005	340
"Demystifying 3D ICs: the pros and cons of going vertical," vol. 22, no. 6, Nov.-Dec. 2006	333
IEEE Transactions on CAD	
"A Unified Approach to Reduce SOC Test Data Volume, Scan Power and Testing Time," vol. 22, no. 3, Mar. 2003	10050
"Modeling of metallic carbon-nanotube interconnects for circuit simulations and a comparison with Cu interconnects for scaled technologies,", vol. 25, no. 1, Jan. 2006	399
"Power modeling and characteristics of field programmable gate arrays," vol. 24, no. 11, Nov. 2005	344
"Active leakage power optimization for FPGAs," vol. 25, no. 3, Mar. 2006.	294
"Modeling of failure probability and statistical design of SRAM array for yield enhancement in nanoscaled CMOS," vol. 24, no. 12, Dec. 2005.	289

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