CEDA

IEEE Council on Electronic Design Automation

IEEE Fellow Nominations

IEEE Fellow is a distinction reserved for select IEEE members whose extraordinary accomplishments in any IEEE field of interest are deemed to merit this prestigious grade elevation. Any person, including non-IEEE members, can nominate someone for the grade of IEEE Fellow.

Nominations are first evaluated by committees in councils and societies, and then by the IEEE Fellow selection committee. To nominate someone for IEEE Fellow who works in the EDA domain, please submit your nomination through CEDA. The deadline for nominations is 1 March 2011.

For more information, please visit this Web site: http://www.ieee.org/membership_services/membership/fellows/index.html

From System to Transistors: A Special Session on Electronic Design Automation of Contemporary VLSI

The Computer-Aided Network Design (CANDE) Committee (http://www.cande.net) is organizing a special session for the 2011 International Symposium on Circuits and Systems. ISCAS 2011 will take place 15-18 May in Rio de Janeiro, Brazil.

CANDE, a technical activity of the IEEE Circuits and Systems Society and CEDA, acts as a working group for electronic CAD. The mission of CANDE is to promote research and best practices for the development and use of CAD software in the design and test of microelectronic circuits and systems.

EDA tools are indispensable for designing contemporary VLSI products. During the past two decades, EDA research has grown from circuit analysis (Spice) to a wide spectrum of topics. These topics range from system-level design to logic synthesis, physical design, timing and logic verification, mixed-signal and analog design automation, and design and manufacturing interfaces.

This special session will include five presentations from academic and industry experts in EDA research. Topics will range from using a system-level design method to reduce operation temperature of multiprocessor SoCs to improving power efficiency by minimizing the number of transistors.

The organizer for this special session is Frank Liu (Austin Research Lab, IBM). The speakers include the following:

- Jaijeet Roychoudhury (Department of Electrical Engineering and Computer Science, University of California, Berkeley);

- Ricardo Reis (Institute of Information, Universidade Federal do Rio Grande do Sul, Brazil);

- David Atienza (Department of Electrical Engineering, École Polytechnique Fédérale de Lausanne, Switzerland);

- Frank Liu (Austin Research Lab, IBM); and

- Farinaz Koushanfar (Department of Electrical and Computer Engineering, Rice University).

Subhasish Mitra (Stanford University), subh@stanford.edu

2010 Computer-Aided Verification Award

This year's Computer-Aided Verification (CAV) Award was presented to Kenneth L. McMillan of Cadence Research Laboratories on 18 July 2010 at the 22nd International Conference on Computer-Aided Verification (CAV 2010).

The annual award, first established by the CAV steering committee in 2008, recognizes a specific fundamental contribution or series of outstanding contributions to the CAV field, and includes a prize of $10,000. This year's prize was presented to McMillan for his sustained contributions to algorithmic verification, and included the citation: "for a series of fundamental contributions resulting in significant advances in scalability of model checking tools."

The Award-Winning Contribution

Algorithmic verification, also called model checking, is a highly successful approach for automatically verifying that a hardware or software system satisfies a given requirement. Many verification tools, academic as well as industrial, have been developed and applied to find subtle bugs in real-world systems.

Nevertheless, the high computational complexity of algorithmic verification remains a central challenge for its application to the ever-growing problems of verification. Over the past 20 years, McMillan has been at the forefront of those trying to meet this critical challenge. He has produced a series of outstanding contributions to the CAV field by suggesting new theories, techniques, and tools for advancing the scalability of model checking.

McMillan's first major contribution was his doctoral dissertation on symbolic model checking, which included an implementation of a symbolic model verifier (SMV) tool and successful applications for finding bugs in industrial cache-coherence protocols. That contribution revolutionized algorithmic verification, but it was merely the start of a long series of major contributions by McMillan to algorithmic verification. This award recognizes those subsequent contributions.

Each of his contributions has significantly influenced both academic research and industry practice, and has dramatically changed the scale of systems that model checking can analyze.

CAV Conference

Computer-aided verification is a subdiscipline of computer science, concerned with ensuring that software and hardware systems operate correctly and reliably. The CAV conference is the premier international conference dedicated to the advancement of the theory and practice of computer-aided formal analysis methods for hardware and software systems. The conference covers the entire spectrum of this field, from theoretical results to concrete applications, with an emphasis on practical verification tools, as well as the algorithms and techniques needed for their implementation.

The CAV conference was founded in 1989 by Edmund M. Clarke, Robert P. Kurshan, Amir Pnueli, and Joseph Sifakis. The first CAV conference was hosted in 1989 in Grenoble, France. Since then, it has been held at multiple sites in North America, Europe, and the Middle East.

CAV 2010 was held 15-19 July in Edinburgh, as part of the Federated Logic Conference.

Orna Grumberg (head of the committee for the 2010 CAV Award)

Papers in IEEE Embedded Systems Letters

The top-five accessed articles from *IEEE Embedded Systems Letters* during July 2010 were as follows:

- "Smartphone-Based Vehicle-to-Driver/Environment Interaction System for Motorcycles," by C. Spelta et al.

- "An FPGA-Based Framework for Technology-Aware Prototyping of Multicore Embedded Architectures," by P. Meloni et al.

- "Hierarchical Additive Hough Transform for Lane Detection," by R.K. Satzoda et al.

- "Embedded Software Design of Scalable Low-Area Elliptic-Curve Cryptography," by M.N. Hassan et al.

- "MPC-on-Chip: An Embedded GPC Coprocessor for Automotive Active Suspension Systems," by Y. Shoukry et al.

Upcoming Conferences (Bill Joyner, william.joyner@src.org)	
ASP-DAC	Yokohama, Japan, 25-28 Jan. 2011
DATE	Grenoble, France, 14-18 March 2011

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