OCTOBER 2008 Currents

CEDA

IEEE Council on Electronic Design Automation

ICCAD 2008

The International Conference for Computer-Aided Design (ICCAD) is for the first time opening its doors to co-located technical workshops. ICCAD's top-tier infrastructure will now also lend support for a number of multi-disciplinary workshops that have been selectively chosen to match ICCAD's rigorous technical program on Thursday November 14.

While ICCAD workshops are independent events with their own paper selection process, they all share the enormous advantage of leveraging ICCAD's professional conference management infrastructure, thereby allowing for an effective workshop management process, and an overall richer experience for every attendee.

The Workshop on Test Structure Design for Variability Characterization is organized by Prof. Hidetoshi Onodera (Kyoto University) and Prof. Dennis Sylvester (University of Michigan). This workshop is motivated by device dimensions in the nanometer regime, and variability as a serious consequential concern. All aspects of test structures will be discussed.

The Electrical-Level Cell Modelling for Timing, Noise, and Power Analysis is organized by Prof. Massoud Pedram (USC) and Dr. Noel Menezes (Intel) as General co-chairs, and Peter Feldman and Igor Keller as Technical co-chairs. The workshop will cover key topics in electrical level modeling.

The Workshop on Compact Variability Modelling is organized by Prof. Kevin Cao (Arizona State University) and Dr. Frank Liu (IBM). This workshop provides a forum to discuss current practice as well as near future research needs in the compact variation modelling, a critical capability to address design driven variability mitigation.

With ICCAD for the first time opening its doors to co-located leading edge technical workshops, in addition –of course- to the strong technical program expected from this premiere conference, the overall ICCAD value for attendees becomes even stronger. See you there!

Sani Nassif. nassif@us.ibm.com and Juan Antonio Carballo juananto@us.ibm.com

Behavioural Synthesis – A Much-needed Second Incarnation?

Reported by Prof. Preeti Ranjan Panda (IIT Delhi)

The seeds of behavioral synthesis (High Level Synthesis – HLS) were sown in the early 80's. This was introduced as a natural step in the automatic generation of digital circuits specified at levels of abstraction higher than the Register Transfer Level (RTL) in hardware description. The essential feature of a *behavioral* description is that, the designer only specifies the high-level behavior of an application, and is asking the synthesis tool to come up with the best *schedule* – decisions about what operations should occur in which clock cycle; a suitable *allocation* – what library elements should be used; and a suggested *binding/mapping* – which operation should be performed on which component (RTL Synthesis also performs allocation/binding, but not scheduling). The behavioral synthesis tool analyses the application, along with any associated constraints, and generates an optimized datapath consisting of instantiations of elements selected from a library and a finite state machine to control it.

Early approaches to solve behavioral synthesis were extensions of the tasks of a compiler. However, there is a vital difference; a compiler targets a fixed architecture, whereas a behavioral synthesis tool also arrives at an application specific architecture. This small conceptual difference results in a very interesting relationship between synthesis and compilers – most compiler optimizations are also applicable in synthesis, but the synthesis problem has its own exciting variants due to the target hardware being decided by the tool itself.

As soon as RTL specification and synthesis began finding acceptance in industrial design flows, engineers naturally began investigating the *next big wave* in automated circuit generation, and behavioral synthesis was a leading candidate in the early 1990s. Product offerings came up by Cadence, Mentor Graphics, and Synopsys. RTL design was itself new but the promised level of productivity leap was not really delivered.

What went wrong? First, a mismatch of expectations. The synthesis tool wanted to automate *every decision* in the behavior, but the designer wasn't quite ready – he wanted

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tight manual control over the generated design. Second, timing closure was hitting the industry even when design entry started at RTL – pre- and post- layout timings were not matching; it could only get worse as we rose higher in the abstraction level. Third, the tools could perhaps have benefited from improved engineering; the user interface was clumsy and the ramp-up time was just too high. Fourth, verification did go for a toss when all actions got rearranged by the tool!

In the early years of the new millennium, the technology, earlier heralded with much fanfare, was quietly all but aborted. Synopsys finally discontinued its Behavioral Compiler and SystemC Compiler products, being the last of the major EDA companies to give up on the technology. High-level synthesis researchers "declared victory" on the topic and moved ahead to even higher levels of abstraction. Somehow, in these new modeling paradigms, the first entry to hardware domain would be RTL – behavioral level was quietly forgotten.

Cut to 2008, and the buzz surrounding this forgotten technology comes as a surprise. Commercial products from both established EDA players and start-ups are now getting traction among designers. Will the second incarnation do better at delivering the mythical productivity boost? Perhaps it will. Clearly, more thought has gone into this round. The interface to the user is different, many working off C/C++/SystemC indicating a changed focus on the end-user. The approach to architecture generation is also more nuanced Research groups haven't really come back in droves, but have branched out into some relevant sub-areas such as timing- and physical awareness.

How does 25 years of behavioral synthesis research get evaluated in terms of its industrial impact? Clearly, the second round of excitement in recent times indicates that one can never write off interesting ideas. The real motivation of behavioral synthesis is too powerful to be overlooked. However, it is also too early to close the research chapter on the technology. Timing closure issues made the first thrust a non-starter, but the problem remains relevant; deep research issues remain to be addressed. Logic synthesis research began in earnest in the late 50's and early 60's, and had to go through its patient wait until the late 80's before finding commercial adoption. Compilers were considered an esoteric technology when the idea of automatic code generation was initially proposed. There is no reason why behavioral synthesis would be exempted from this circuitous route. These are still early days. The real *wave* is patiently awaited.

Preeti Ranjan Panda (panda@cse.iitd.ac.in)

Moving Ahead with Josephson Computation

Reported by Prof. Theodore Van Duzer (University of Berkeley)

Recent industry trends clearly establish that design tradeoffs have brought CMOS close to the limits of its scalability. The US government is supporting work to address the fundamental question of a substitute for silicon (CMOS) in very high-end computing (HEC) environments. Although microprocessor firms have turned to parallel multiple cores, many demanding applications require higher-performance components.

A government-sponsored study explored the potential for superconducting ultra-high clock-speed (50 GHz or higher) single-flux-quantum processing, along with the associated memory, fabrication, and packaging. The report indicated that a large five-year project would be required. A precursor to the five-year project is being supported this year with several groups funded to do preparatory research for the five-year project.

Wholly superconducting memory remains an important target so that it can be on the chip with the processor and work at clock rates as close as possible to the processor clock rate, but at the University of California, Berkeley, we are following up research on our hybrid Josephson-CMOS second-level 4 kelvin memory. The storage is in compact nonvolatile CMOS cells with very low-power-dissipation superconducting interface circuits. In a collaborative project with Yokohama National University, we have brought the work to the point of measuring the access time (500 ps) for a single bit in a 64-kbit CMOS array. Our goal for this year is to determine the access time of a 64-kbit memory into which complete words can be written at arbitrary locations and then subsequently read. Such a hybrid will be able to take advantage of advances in CMOS technology, such as higher density, faster operation, and lower voltages, and can readily be scaled to larger capacities.

Theodore Van Duzer. vanduzer@eecs.berkeley.edu

***Upcoming Conferences/** Bill Joyner, william.joyner@src.org*	
VLSI-SOC	Rhodes (Greece), Oct. 13-15, 2008
ESWEEK	Atlanta (USA), Oct. 19-24, 2008
ICCAD	San Jose (USA), Nov. 10-13, 2008
FMCAD	Portland (USA), November, 2008
ASP-DAC	Yokohama (Japan), Jan. 19-22, 2009

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