October 2011 Currents

IEEE Council on Electronic Design Automation

ARCS 2012 Call for Papers

The 2012 International Conference on Architecture of Computing Systems (ARCS) will take place on 28 February to 2 March in Munich. This year's conference will focus on platforms for embedded computer systems.

Authors are invited to submit original, unpublished research papers on one of the following topics:

- architectures and design methods or tools for robust, failure-tolerant, real-time embedded systems;
- cyberphysical systems and distributed-computing architectures;
- multi- or many-core architectures, memory subsystems, and communication architectures for reliable systems;
- tool support for many-core systems, including programming models, runtime systems, middleware, and verification;
- generic and application-specific accelerators for multi-core architectures; and
- adaptive system architectures, such as reconfigurable systems in hardware and software.

After the conference, authors of selected papers will be invited to submit an extended version of their contribution for publication in a special issue of the *Journal of Systems Architecture*.

In addition, a best paper and best presentation award will be presented at the conference.

For more information, go to http://www.arcs2012.tum.de.

TAU 2012 Power Grid Contest

In light of the success of the Power Grid Simulation Contest at the 2011 ACM/IEEE International Conference on Timing Issues (TAU), there will be a second contest at TAU 2012, which will take place on 18-20 January 2012 at National Taiwan University.

In the 2011 contest, each team performed a DC solution for a given power grid network, and the evaluation was based on accuracy, memory, and speed on a single-core machine. This year, the focus will be on transient solutions and parallel implementations.

IBM's Raju Balasubramanian, Frank Liu, and Zhuo Li will administer the contest. A set of four to eight benchmark circuits will be used to evaluate the tool from each team. These benchmarks will also define the input and output formats for evaluating transient solutions.

Participants are encouraged to explore parallel implementations of the simulation algorithms. Once again, the contest machine will run on Linux and GCC.

The evaluation metrics will be based on three factors: CPU time; memory usage; and solution accuracy.

Please be sure to visit the TAU website (http://www.tauworkshop.com) for updates, including metrics to evaluate the parallel algorithm and transient solutions, as well as detailed information on software versions, CPU speed and memory, and other configuration information. Please send all emails regarding the contest to taucontest2011@gmail.com (and add "TAU2012_contest" to the subject line of your message).

For more information, go to http://www.tauworkshop.com.

FAC 2011

The Frontiers in Analog Circuit (FAC) Synthesis and Verification Workshop, colocated with the 23rd International Conference on Computer Aided Verification (CAV), took place at Snowbird, Utah, on 14-15 July 2011.

This workshop partly originated from the Formal Verification of Analog Circuits (FAC) Workshop, which was held in Edinburgh in 2005, Princeton in 2008, and Grenoble in 2009.

Inspired by discussions at an Intel analog and mixed-signal workshop and a Dagstuhl seminar in July 2010, the organizers decided to broaden the range of analog-design automation topics covered at the FAC workshop. In particular, this year's workshop included both formal methods and simulation-based verification and analog synthesis, as reflected in the workshop name change.

FAC 2011 was organized by Program Chairs Chris Myers (University of Utah) and Kevin Jones (City University London), along with a diverse program committee comprising both academic and industrial representatives. The

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IEEE Circuits and Systems Society and IEEE Microwave Theory and Techniques Society were the technical sponsors. The workshop also received generous support from CEDA as well as Intel, which provided partial support for the invited speakers and increased student participation.

The workshop attracted 41 registered participants. The program included six excellent invited speakers—Robert Hum (Mentor Graphics), Gregory Taylor (Intel), Mihai Marcu (Agilent Technologies), Mark Horowitz (Stanford University), Rob Rutenbar (University of Illinois at Urbana-Champaign), and Christoph Grimm (Vienna University of Technology)—as well as an industrial panel session.

There were also 21 short talks presented by those who contributed abstracts, covering a range of topics, including modeling, synthesis, assertion languages, simulation, analysis, and formal verification. Each session concluded with a panel discussion by all speakers, which helped make this a lively, dynamic meeting.

A discussion session at the end of the workshop decided to meet next as a colocated workshop with the 2013 IEEE International Solid-State Circuits Conference (ISSCC), which will take place on 17-21 February in San Francisco.

For more information, go to http://www.async.ece.utah.edu/FAC2011.

Early Career Award

In 2009, CEDA established the first Early Career Award. This award recognizes an individual who has made innovative and substantial technical contributions to the area of electronic design automation (EDA) in the early stages of his or her career.

These contributions are measured in relation to the nominee's technical merit and creativity in performing research, and are assessed on the basis of the individual's published record and the references accompanying the nomination. The award is intended to be equally available to contributors from academia and industry.

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The first Early Career Award was given in 2009 to Igor Markov (University of Michigan). In 2010, the award went to Luca Daniel (Massachusetts Institute of Technology).

In 2011, the Award Committee, after evaluating the current and potential impact of the nominees' individual contributions to EDA, decided to present the award to Valeria Bertacco (University of Michigan–Ann Arbor) for her exceptional contributions in hardware verification—in particular, her work on semiformal verification, runtime and postsilicon verification, and correctness-constrained execution.

This award will be presented on 7 November at the opening session of the 2011 International Conference on Computer-Aided Design (ICCAD) in San Jose, California.

Papers in IEEE Embedded Systems Letters

The top-five accessed articles from *IEEE Embedded Systems Letters* in June 2011 were as follows:

- "Island-Based Adaptable Embedded System Design," by I. Beretta et al.
- "A Dynamic Resource Management and Scheduling Environment for Embedded Multimedia and Communication Platforms," by A. Bahga et al.
- "Lossless Hyperspectral Image Compression System-Based on HW/SW Codesign," by Y.-T. Hwang et al.
- "Scalable Many-Domain Power Gating in Coarse-Grained Reconfigurable Processor Arrays," by D. Kissler et al.
- "Custom Microcoded Dynamic Memory Management for Distributed On-Chip Memory Organizations," by I. Anagnostopoulos et al.

Upcoming Conferences (Sani Nassif,, sani.nassif@gmail.com)	
FMCAD	Austin, Texas, 30 Oct.-2 Nov. 2011
ICCAD	San Jose, Calif., 6-10 November 2011

IEEE Embedded Systems Letters *is open for submissions. Visit mc.manuscriptcentral.com/les-ieee*

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