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Currents

CEDA

IEEE Council on Electronic Design Automation

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ICCAD 2020 – Call for Participation

The 39th edition of the International Conference on Computer Aided Design (ICCAD 2020) will take place November 2-5, 2020. This year, due to the global COVID-19 pandemic, many conferences are forced to make the event work in the online world. Consequently, the ICCAD 2020 Executive Committee decided to move forward with a virtual conference due to the continued uncertainty surrounding the COVID-19 situation. Nevertheless, we are very excited to test out this new online edition for the first time in ICCAD's 39-year history. Even though the virtual events lack the kind of interpersonal communications attendees get from in-person events, a much lower registration fee with no travel overheads may boost the number of participants. Also, a carefully tuned schedule with a virtual platform can make it a true "global" event for anyone around the world to attend ICCAD 2020. For registration rates and to register, please visit https://iccad.com/registration-rates

SLIP^2 – Call for Participation

The 2020 ACM/IEEE International Workshop on System-Level Interconnect Problems and Pathfinding (SLIP^2) is the 22nd, "rebooted" edition of the System-Level Interconnect Prediction (SLIP) Workshop and will take place online on November 5, 2020. As computing systems and applications grapple with a post-Moore, post-CMOS, post-von Neumann future, fundamental interconnect problems and pathfinding challenges have become more critical to address than ever before.

SLIP^2, co-located with ICCAD 2020, will bring together researchers and practitioners who have a shared interest in the challenges and futures of system-level interconnect, coming from wide-ranging backgrounds that span system, application, design and technology. The technical goals of the workshop are to (1) identify fundamental problems, and (2) foster new pathfinding of design, analysis, and optimization of interconnect and communication fabrics in electronic systems. A special emphasis this year is on predictive system interconnect modeling technologies, and on novel interconnect technologies and architectures for a beyond-Moore era. Additionally, a more interactive, workshop-like tone and format - recalling earlier editions of the SLIP workshop - is a goal for SLIP^2 this year. To register and participate, please visit the conference website.

MLCAD Workshop – Call for Participation

The second ACM/IEEE Workshop on Machine Learning for CAD (MLCAD) will take place virtually on November 16-20, 2020. The virtual MLCAD workshop focuses on Machine Learning (ML) methods for all aspects of CAD and electronic system design. The predecessor of this workshop series was held at the Design, Automation and Test in Europe (DATE) Conference in March 2019, followed by the inaugural regular workshop in Banff, Canada, in September 2019. The workshop is sponsored by both IEEE Council on Electronic Design Automation (CEDA) and ACM Special Interest Group on Design Automation (SIGDA).

Advances in ML over the past half-dozen years have revolutionized the effectiveness of ML for a variety of applications. However, design processes present challenges that require parallel advances in ML and CAD as compared to traditional ML applications such as image classification. As such, the purpose of the workshop is to discuss, define and provide a roadmap for the special needs for ML for CAD where CAD is broadly defined as design-time techniques as well as run-time techniques. Topics of interest to this workshop include but are not limited to: ML for system-level design, ML approaches to logic design, ML for physical design, ML for analog design, ML for power and thermal management, ML for Design Technology Co-Optimization (DTCO), ML methods to predict aging and reliability, labelled and unlabelled data in ML for CAD, ML techniques for resource management in many cores, and ML for verification and validation. To register, please visit the workshop website.

TAU 2021 – Call For Contributions

The ACM International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems will take place April 8-9 2021. The TAU series of workshops provide an informal forum for practitioners and researchers working on these and other temporal aspects of analog and digital systems to disseminate early work and engage in a free discussion of ideas. On the thirty-first anniversary of the Tau series, the Tau 2021 workshop invites submissions and proposals from the traditional as well as emerging areas related to the timing properties of digital electronic systems, including but not limited to the following topics: Timing (including incremental timing), modeling and simulation, variability, power, trade-offs and optimization, clocking and characterization, and emerging Ttechnologies. All papers (including invited papers and camera-ready versions) must be submitted electronically here.

ASP-DAC 2021 – Call for Participation

ASP-DAC 2021 is the 26th annual international conference on VLSI design automation in Asia and South Pacific regions, one of the most active regions of design and fabrication of silicon chips in the world and will take place as a virtual conference January 18-21, 2020. The conference aims at providing the Asian and South Pacific CAD/DA and design community with opportunities of presenting recent advances and with forums for future directions in technologies related to Electronic Design Automation (EDA). The format of the meeting intends to cultivate and promote an instructive and productive interchange of ideas among EDA researchers/developers and system/circuit/device designers. All scientists, engineers, and students who are interested in theoretical and practical aspects of VLSI design and design automation are welcomed to ASP-DAC. To register for the conference, please visit the conference website.

DATE 2021 – Call for Participation

The 24th Design Automation Test in Europe (DATE 2021) Conference and exhibition is the premiere European event, bringing together designers and design automation users, researchers, and vendors, as well as specialists in the hardware and software design, test and manufacturing of electronic circuits and systems. DATE 2021 will be held as a virtual event February 1-5, 2021. DATE 2021 puts a strong emphasis on both technology and systems, covering ICs/ SoCs, reconfigurable hardware and embedded systems, and embedded software. To participate and register, please visit the conference website.

Papers in IEEE Embedded Systems Letters

The top-five accessed articles from *IEEE Embedded Systems Letters* in September 2020 were as follows:

- "A Safe, Secure, and Predictable Software Architecture for Deep Learning in Safety-Critical Systems," by A. Biondi *et al.,*
- "Virtio Front-End Network Driver for RTEMS Operating System," by J.H. Kim and H.-W. Jin
- "Embedding Encryption and Machine Learning Intrusion Prevention Systems on Programmable Logic Controllers," by T. Alves, R. Das, and T. Morris
- "Iterative Histogram-Based Performance Analysis of Embedded Systems," by B. Dreyer, C. Hochberger, T. Ballenthin, and S. Wegener
- "Do Not Trust, Verify: A Verifiable Hardware Accelerator for Matrix Multiplication," by M. I. M. Collantes and S. Garg.

Papers in IEEE Design & Test Magazine

The top-five accessed articles from *IEEE Design & Test Magazine* in September 2020 were as follows:

- "Approximate Computing: A Survey," by Q. Xu, T. Mytkowicz, and N. S. Kim
- "Robust Machine Learning Systems: Challenges,Current Trends, Perspectives, and the Road Ahead," by M. Shafique *et al.,*
- "Security and Privacy in Cyber-Physical Systems: A Survey of Surveys," by J. Giraldo *et al.*,
- "The Impact of Ferroelectric FETs on Digital and Analog Circuits and Architectures," by X. Chen *et al.,*
- "Scan Integrity Tests for EDT Compression," by W.-T. Cheng *et al.*

IEEE Embedded Systems Letters **is open for submissions.**
Visit ieee-ceda.org/publication/esl-publication/author-guidelines

IEEE Design & Test **is open for submissions.**
Visit https://ieee-ceda.org/publication/ieee-design-test-dt/paper-submission-instructions

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