June 2021 CEDA Currents
IEEE Council on Electronic Design Automation

Call for Submissions: ACM SIGDA/IEEE CEDA Ph.D. Forum at DAC 2021

The Ph.D. Forum at the 2021 Design Automation Conference is a poster session sponsored by ACM SIGDA and IEEE CEDA for Ph.D. students to present and discuss their dissertation research with people in the EDA community. The forum has become one of the premier fora for Ph.D. students in design automation to receive feedback on their research and for industry to see academic work in progress. Hundreds of people attended past fora. Participation in the forum is competitive with acceptance rate of around 30%.

Limited funds will be available for travel assistance, based on financial needs. The forum is open to all members of the design automation community and is free-of-charge. DAC registration is not required in order to attend this event. Abstracts are due July 20. For more information, visit here.

CAD for Assurance Webinar: Side-Channel Analysis and MIMI

IEEE CEDA's Hardware Security and Trust Technical Committee (HSTTC) developed the "CAD for Assurance" website and tools for faculty, students, post docs, and practitioners in the hardware security community to disseminate their work. This initiative also includes a series of monthly, virtual webinars.

The next webinar is June 11 at 11:00 AM-12:20 PM ET. Debdeep Mukhopadhyay (IIT Kharagpur) will present Side-Channel Analysis. Patanjali SLPSK and Jonathan Cruz (University of Florida) will present MIMI.

Registration is required. For more information on this webinar series and to register, visit the CEDA website.

Call for Contributions: IEEE Transactions on Computers – Special Issue on Software, Hardware and Applications for Neuromorphic Computing

Inspired by biological neural systems, neuromorphic computing has drawn much attention for its great potential of achieving machine intelligence at extremely low energy dissipation. Bio-inspired computing models have been investigated for information encoding, sparse representation, event driven communication/computation, and online learning. This new computing paradigm triggered a recent wave of innovations in software and hardware architecture and emerging device technology, which consequently enabled many novel applications.

This special issue of IEEE Transactions on Computers will explore academic and industrial research on all topics related to neuromorphic computing, from computing model, software and hardware architecture to application design.

Guidelines concerning the submission process and LaTeX and Word templates can be found here. While submitting through ScholarOne, please select this special issue/section option. Submissions are due October 15.

Call for Participation: CEDA Virtual Distinguished Lecturer Webinar Series

The Virtual Distinguished Lecturer Program allows us to continue to serve the CEDA participants and the electronic design automation community the opportunity to hear from our respected Distinguished Lecturers.

David Pan (University of Texas at Austin) will present Closing the Virtuous Cycle of AI for IC and IC for AI on June 24 at 11:00 AM – 12:00 PM ET. Registration is free but required via Zoom.

The recent artificial intelligence (AI) boom has been primarily driven by three confluence forces: algorithms, data, and computing power enabled by modern integrated circuits (ICs), including specialized AI accelerators. This talk will present a closed-loop perspective for synergistic AI and agile IC design with two main themes, AI for IC and IC for AI. As semiconductor technology enters the era of extreme scaling, IC design and manufacturing complexities become extremely high. More intelligent and agile IC design technologies are needed than ever to optimize performance, power, manufacturability, design cost, etc., and deliver equivalent scaling to Moore's Law.

This talk will present some recent results leveraging modern AI and machine learning advancement with domain-specific customizations for agile IC design and manufacturing closure. Meanwhile, customized ICs, including those with beyond-CMOS technologies, can drastically improve AI performance and energy efficiency by orders of magnitude. I will present some recent results on hardware/software co-design for high performance and energy-efficient optical neural networks. Closing the virtuous cycle between AI and IC holds great potential to advance the state-of-the-art of each other significantly.

Call for Contributions: IEEE Journal on Exploratory Solid-State Computational Devices and Circuits – Special Issue on

Emerging Hardware for Cognitive Computing

Using CMOS, emerging resistive memories, and other device types as the basis, neuromorphic computing is innovating vertically from devices, to circuits, to systems to re-define how computation can be done. Looking forward, the realm of "cognitive computing" is inspired by new and continually emerging understanding of advanced brain and neuronal behavior that enables efficient and real-time learning and reaction.

This call for papers is on emerging hardware for cognitive computing. The focus and emphasis of these special topic papers is beyond DNN processing, as well as beyond multi-weight synapses and basic neuron integrating, firing, and stochasticity.

The submission deadline for this special issue is on July 15. Submission guidelines can be found here.

ACM Transactions on Design Automation of Electronic Systems – Special Issue on High-Level Synthesis for FPGA: Next-Generation Technologies and Applications

Due to the end of Dennard scaling and Moore's law, complex hyper-pipelined processors are increasingly replaced by heterogeneous System-on-Chip (SoC) architectures with many specialized components. FPGA devices are becoming common targets for these systems since they allow fast turn-around time, field upgradability, and easy deployment of hardware/software solutions. To cope with the increasing complexity of such systems, designers need to raise the abstraction level from custom design flows to high-level approaches. High-level synthesis (HLS) is a popular method that allows designers to describe the functionality of a component at the software level and automatically generate the corresponding hardware description, reducing the gap between application and hardware designers. Since HLS has been making a great amount of progress and an increasing number of different application domains are pushing designers towards hardware acceleration, HLS is becoming a key enabling technology for FPGA design.

Submissions for this special issue are due by June 30. Submissions should be made through the ACM TODAES submission site and formatted according to TODAES author guidelines.

IEEE CEDA System Validation and Debug Technology Committee Presents New Standard

IEEE System Validation and Debug Technology Committee (SVDTC) (Debug Subcommittee) has prepared a presentation to IEEE to approve Scan and Array Debug Standardization efforts. The committee presented to IEEE Test Technology Standards Committee a proposal to approve starting a new IEEE Standards effort for "Scan and Array Debug for SoCs". This topic was titled as "Standard for System-level State Extraction for Functional Validation and Debug".

Sankaran Menon, Chair of the SVDTC Debug sub-committee presented the Project Authorization Request for P2929 "Standard for System-level State Extraction for Functional Validation and Debug" to the IEEE TTSC and the Standardization effort was approved by TTSC. Sankaran Menon started the IEEE P2929 standardization WG meetings with about 28 attendees from Academia and Industry mid-December 2020.

If you are interested in participating, contact Sankaran Menon PhD at smenon@ieee.org or Sankaran.Menon@gmail.com.

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Please send contributions to Vasilis F. Pavlidis

Contributions Form

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IEEE Embedded Systems Letters is open for submissions

Visit http://bit.ly/ESLSubmissions

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