October 2021 Currents

CEDA®

IEEE Council on Electronic Design Automation

Congratulations to the 2021 A. Richard Newton Technical Impact Award in Electronic Design Automation Recipients

The Newton Award annually honors a person or persons for an outstanding technical contribution within the scope of electronic design automation, as evidenced by a paper published at least ten years before the presentation of the award.

This year John A. Waicukauski, Eric Lindbloom, Barry K. Rosen, and Vijay S. Iyengar were selected for their paper "Transition Fault Simulation."

For more information on this award and all IEEE CEDA awards or to submit a nomination, please visit our website.

Call for Participation: Embedded Systems Week 2021

Embedded Systems Week (ESWEEK) is the premier event covering all aspects of hardware and software design for smart, intelligent, and connected computing systems. The virtual conference will run from 8-15 October 2021 and brings together three conferences (CASES, CODES+ISSS, EMSOFT), a special track on Trustworthy IoT (Internet of Things), a symposium (NOCS), and several workshops and tutorials. ESWEEK allows attendees to benefit from a wide range of topics covering the state of the art in embedded systems research and development.

The lightning talk videos, paper PDFs, and asynchronous Q&A channels for all the papers associated with the three; CASES, CODES+ISSS, and EMSOFT are now available through Whova.

The ACM TECS Special Issue with all journal-track papers can be also accessed here. All articles will be available to download after the conference.

Registration is still open and can be accessed here. A limited number of attendee registration fee waivers for attendees with demonstrated need are available. For more information on ESWEEK, visit the conference website.

Call for Participation: Design Automation Conference 2021 Registration Now Open

The Design Automation Conference (DAC) is recognized as the premier conference for design and automation of electronic systems. DAC offers outstanding training, education, exhibits, and superb networking opportunities for designers, researchers, tool developers, and vendors.

DAC 2021 will be a hybrid conference hosted in-person at the Moscone Center in San Francisco, CA, USA (5-9 December) and virtually (7-10 December). To receive advanced registration rates for DAC 2021, register by 20 November on the DAC website. A full list of rates and included activities can be found here.

For those attending in person, please refer to the local California Department of Health COVID-19 precautions and requirements.

Call for Papers: Design, Automation and Test in Europe 2022

The 2022 Design, Automation and Test in Europe Conference (DATE) is pleased to present a special hybrid format for its 2022 event, as the situation related to COVID-19 is improving but safety measures and restrictions will remain uncertain for the upcoming months across Europe and worldwide.

In transition towards a future post-pandemic event again, DATE 2022 will host a two-day live event in presence in the city of Antwerp (just north of Brussels in Belgium) 14-15 March 2022, to bring the community together again, followed by other activities carried out entirely online 16-23 March 2022. This setup combines the in-presence experience with the opportunities of on-line activities, fostering the networking and social interactions around an interesting program of selected talks and panels on emerging topics to complement the traditional DATE high-quality scientific, technical, and educational activities.

Ph.D. Forum, Multi-Partner Projects, University Fair, and Young People Program submissions are due on 15 November 2021. All deadlines are strict and no extensions will be given. Please visit the conference website to download the call for papers for descriptions and submission instructions.

ITC-Asia Went Virtual in 2021

The 5th IEEE International Test Conference in Asia (ITC-Asia) was held virtually on 18-20 August 2021.

The three-day technical program featured two, half-day tutorials (by Yervant Zorian and Adit Singh), six keynote speeches (by Shaojun Wei, Xinli Gu, Qiang Xu, Tim Cheng, Krishnendu Chakrabarty, and Norman Chang), nine regular research paper presentations, 12 industrial talks, and 17 invited speeches in the special sessions. There were 230 participants from 11 countries and regions registered.

The ITC-Asia 2021 Cadence Best Paper Award went to paper "Automatic Test Program Generation for

Transition Delay Faults in Pipelined Processors" by Kai-Hsun Chen, Bo-Yi Yang, Jia-Ruai Liang, Hung-Lin Chen, and Jiun-Lang Huang from National Taiwan University.

The conference was sponsored by IEEE CEDA, China Computer Federation (CCF), Tongji University, IEEE Computer Society, and IEEE Test Technology Technical Council (TTTC), incorporated with IEEE Hardware Security and Trust Technical Committee (HSTTC) and CCF Fault Tolerant Computer Technical Committee (FTCTC).

For more information, please visit the ITC-Asia 2021 conference website. Conference papers and recorded presentations are now available for registered attendees.

CAD for Assurance Panel: Security Assessment and Verification for Microelectronics - A New Future or More of the Same?

IEEE CEDA's Hardware Security and Trust Technical Committee (HSTTC) developed the "CAD for Assurance" website and tools for faculty, students, post docs, and practitioners in the hardware security community to disseminate their work. This initiative also includes a series of monthly, virtual webinars.

The next panel presentation "Security Assessment and Verification for Microelectronics - A New Future or More of the Same?" by Kevin Bush (MIT Lincoln Lab), Sharad Malik (Princeton), Keith Rebello (Darpa), Robert B. Jones (Intel), Jamin McCue (AFRL) is 8 October at 11:00 AM - 12:20 PM ET.

Registration is required. For more information on this webinar series and to register, visit the CEDA website.

Call for Participation: Complete the IEEE ESL and IEEE D&T Surveys

IEEE Embedded Systems Letters and the IEEE Design&Test (D&T) want to hear from you! Please complete the feedback surveys for ESL and D&T. Your feedback is important to the future success of these journals.

If you have any questions regarding the surveys, please contact us at admin@ieee-ceda.com.

Call for Papers: IEEE Design&Test Special Issue on Design and Test of Multi-Chip Packages

From auspicious beginnings over 10 years ago, the promise of 3D-IC has begun to turn the corner to more popular usage. This D&T Special Issue on Multi-Chip Packages focuses exclusively on design and design-for-test for the three dimensional, chiplet-based, and stacked ICs, based on through-silicon vias (TSVs), micro-bumps, and/or interposers. While these stacked ICs offer many attractive advantages with respect to heterogeneous integration, small form-factor, high-bandwidth and performance, and low-power dissipation, there are many open issues with respect to designing and testing such products.

This special issue seeks original manuscripts that will cover innovative research and practical applications for the testability and design challenges on both pure 3DIC implementations, as well as, other multi-chip packaging implementations, including chiplets, active and passive interposers.

The deadline to submit manuscripts has been extended to 15 October 2021. For a full list of topics, important dates, and guest editors, visit our website.

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Please send contributions to Vasilis F. Pavlidis

Contributions Form

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IEEE Embedded Systems Letters is open for submissions

Visit bit.ly/ESLsubmissions

IEEE Design & Test is open for submissions

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