IEEE Design&Test

Call for Papers for a Special Issue on

Special Issue on Open-Source Silicon

Aim and Scope

Since the launch of the Open MPW program by Google, SkyWater, and Efabless in 2020, we have witnessed a steady expansion of the open-source IC design ecosystem. There are more than 5,500 users on the open-silicon Slack space and nearly 1,000 design projects have been initiated on Efabless' project portal. In addition to SkyWater's 90 and 130 nm offerings, designers can now also target open PDKs by Globalfoundries (180 nm) and IHP (130 nm BiCMOS). These efforts have resulted in hundreds of tapeouts across 12 shuttle runs that are now beginning to yield measured silicon results.

Several motivators underpin this new movement, primarily related to the lack of sharing and reproducibility in the current ecosystem that builds on nondisclosure agreements. By embracing the open-source approach and promoting transparency, the new ecosystem fosters reproducibility and reuse by providing a complete open chain of tools, design kits, and design libraries. It will allow designers to collaborate openly, share knowledge, and work collectively toward enhanced reliability and productivity. It also grants broader access to IC design beyond the electrical engineering field, benefiting educational institutions, research organizations, and facilitating innovative cross-disciplinary projects. Lastly, the new ecosystem enables the utilization of open data for training AI-based generators, leading to significant advancements in design methodology.

The goal of this special issue is to disseminate the most exciting open-source silicon results to date and to promote further interest in open-source chip design. We invite the community to submit contributions that are primarily focused on circuit design and measured results (as opposed to design tools, which were the topic of a past issue). A requirement for all contributions is that the circuits were designed exclusively using open-source tools and PDKs. ● Emerging technology (RRAM, unconventional uses & integration, etc.)

Topics of Interest

We primarily invite contributions showing measured silicon results. Exceptionally strong submissions conveying design insights and simulation results may also be considered. Areas of interest include, but are not limited to:

- Digital circuits
- Power management

- Analog/mixed-signal & RF
- Emerging technology (RRAM, unconventional uses & integration, etc.)

Submission Guidelines

Prospective authors should follow the submission guidelines for IEEE Design & Test. All manuscripts must be submitted electronically to the IEEE Manuscript Central Web site at https://mc.manuscriptcentral.com/dandt. Please select manuscript type ''SI: Open-Source Silicon'' from the dropdown menu when submitting. All articles will undergo the standard IEEE Design & Test review process. Submitted manuscripts must not have been previously published or currently submitted for publication elsewhere. Manuscripts must not exceed 5,000 words, including figures (with each average-size figure or table counting as 200 words) and a maximum of 12 References (50 for surveys). This amounts to about 4,000 words of text and a maximum of five small to medium figures. Accepted articles will be edited for clarity, structure, conciseness, and grammar, passive to active voice, logical organization, readability, and adherence to style. Please see IEEE Design & Test Author Information at: https://ieee-ceda.org/publication/ieee-design-test-dt/author-info.

Schedule

- Open for submissions   : September 25, 2023
- **Submission deadline : November 30, 2023**
- Notification First Round : February 15, 2024

- Revision submission   : April 30, 2024
- Final decisions   : June 15, 2024
- Tentative publication   : Fall 2024

Guest Editors

Kwantae Kim, ETH Zurich, Switzerland
Francisco Brito Filho, Fed. Univ. Semiárido, Brazil
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