IEEE Design & Test

Call for Contributions

Special Issue on "Computing in the Dark Silicon Era"

Supply voltage scaling has slowed down for leakage dominated nanometer transistors. As a result, although we can continue to integrate more transistors per unit area with technology scaling, the power per transistor has not been scaling commensurately. Coupled with the physical limits imposed by device packaging and cooling technology on the peak power and peak power density, this results in the so-called *dark silicon problem*. That is, the entire chip cannot be simultaneously powered-on (at nominal voltage/frequency) for a given thermal design power (TDP) constraint and thus must stay *dark* (i.e., power-gated). Early studies by various academic and industrial researchers have projected that at the 7 nm technology node, more than 50% of the chip area will stay dark.

The dark silicon problem introduces new challenges for the design, architecture, and test communities concerning various design abstractions. For instance, how to best utilize the abundance of (potentially dark) transistors, both in terms of design time provisioning and run-time management, *so as to improve quality metrics (like performance and reliability) within peak power and thermal constraints*. Dark Silicon processors are envisaged to be designed different from the largely homogeneous multi-cores commercially available today, and will instead feature a *heterogeneous mix of computing and communication resources* to achieve higher performance and better power/energy/thermal efficiency. An evidence of this trend is the *heterogeneous system architecture* (HSA) which is becoming the norm for different computing platforms, including servers and mobile devices.

The objective of this special issue is to provide a forum for academic and industry researchers to publish new research results that solve the outstanding challenges posed by the dark silicon problem.

Topics of interest include, but are not limited to:

(1) Exploiting new architectural opportunities in next generation dark silicon chips including but not limited to heterogeneous, reconfigurable, GPU, and application-specific design paradigms and industrial trends.

(2) Efficient and scalable run-time dark silicon management under power and thermal considerations while jointly optimizing for quality metrics including performance, reliability, lifetime, etc.

(3) Opportunities and challenges for dim silicon (e.g. using near-threshold voltage computing) including analysis, modeling, variability and reliability challenges.

(4) Turbo Boosting for computation and communication resources.

(5) Hardware/Software co-synthesis and implementation issues on Heterogeneous System Architecture (HSA).

(6) Programming models (OpenCL, CUDA), compiler and operating system support for dark silicon chips with specialized resources, adaptive modes of parallelism, etc.

(7) On-chip communication architectures for dark silicon chips, e.g., efficient data transfer mechanisms between different parts of the chip.

(8) Integration of new device and cooling technologies and *their interaction with dark silicon*.

(9) Killer application domains (mobile, big data, enterprise, etc.) and accelerator architectures.

Submission Guidelines:

Guidelines for DnT paper are given at: http://ieee-ceda.org/publications/d-t/paper-submission

Please choose the special session category "DarkSilicon-SI" while submitting the manuscript to the ScholarOne Manuscripts website (https://mc.manuscriptcentral.com/dandt).

Paper Submission and Review Schedule:

Submission Deadline:	31 January 2016
First Round of Reviews:	31 March 2016
Revisions Due:	01 June 2016
Notification of Final Acceptance:	15 July 2016
Camera Ready Due:	30 July 2016

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