IEEE Journal on Exploratory Solid-State Computational Devices and Circuits

Special Topic on 3D Logic and Memory for Energy Efficient Computing

CALL FOR PAPERS

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Aims and Scope

Monolithic microelectronic design is facing tremendous challenges in the growing need of computation memory bandwidth and latency, and the energy efficiency of computation which is limiting its performance and cost. Although recent advances (e.g., domain-specific acceleration, near-memory and in-memory computing techniques) try to address these issues, the scaling trend of monolithic design still lags behind the ever-increasing demand of AI algorithms, high-performance computing, high-definition sensing and other data-intensive applications. In this context, technological innovations, in particular 3D integration through packaging and monolithic methods, are critical to enabling heterogeneous integration (HI) and bringing significant performance, energy and cost benefits beyond traditional chip design. 3D logic and memory design allow heterogeneous functional macros (i.e. chiplets) to be flexibly produced and connected with higher interconnection density, length reduction and area utilization, opening new opportunities across the microelectronic design stack.

The paradigm shift to heterogeneous integration and monolithic 3D methods requires a tight collaboration between packaging and chiplet designs spanning the entire design cycle, including devices, circuits, architectures, and design automation tools. Logic and memory will be partitioned into various 3D modules. The designers need to customize each module and define the interface, and assess system-level tradeoffs in performance, data movement, and energy efficiency. Design and synthesis tools have to be aware of 3D integration and planning knowledge (e.g., power delivery, heat dissipation and reliability) to enable the packaging and chiplet co-design. Furthermore, early predictive modeling and analysis of the 3D HI circuits and systems are essential to minimize the iteration cost between 3D architecture definition and design implementation.

This special issue of the IEEE Journal on Exploratory Computational Devices and Circuits (JXCDC) aims to call for the recent research advances in the area of 3D logic and memory design

spanning from monolithic 3D and advanced packaging technology to circuits and architectures. Papers on co-design and optimization across multiple domains are encouraged.

Topics of Interests

Prospective authors are invited to submit original works and/or extended works based on conference presentations on various aspects of 3D logic and memory design for energy efficient computing. Topics of special interest include but are not limited to:

- Technology perspectives of 3D heterogeneous integration
- Emerging monolithic 3D logic and memory devices to improve energy efficiency of computation.
- Advanced packaging for 2.5D and 3D integration to improve energy efficiency of computation.
- Logic design and partition for a 3D system
- Network topology for 3D data movement
- 3D memory design and architectures to reduce the power consumption of data movement.
- Signaling interface cross 3D modules
- Thermal cooling and management to address the increased power density of 3D integration.
- Power delivery, thermal management and reliability of 3D integrated circuits
- Power delivery, thermal management and reliability of 3D integrated circuits
- Architectural innovations for energy-efficient 3D HI
- Prototypes of multi-tier logic and memory macros
- EDA tools for multi-domain 3D integration

Information on **submission guidelines** can be found at the JxCDC page on the SSCS website.

Paper submissions must be done through the IEEE Author Portal website:
https://ieee.atyponrex.com/journal/JXCDC

Important Dates
Open for Submission: February 15th, 2024
Submission Deadline: May 31st, 2024
First Notification: June 30th, 2024
Revision Submission: July 15th, 2024
Final Decision: July 31st, 2024
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