

IEEE Design&Test

Call for Papers for a Special Issue on Approximate Test

Aim and Scope

Increasing demands for safety and reliability require that tests be used to screen for all possible Time 0 and latent defects. On the other hand, cost and silicon shipment throughput constraints require an approach of minimal and adaptive test. We have known that product manufacturing teams have compelling test quality improvement and test cost reduction targets, which often appear to get more challenging and dichotomic, e.g. better test screens at lower cost.

Towards meeting these targets, test methods have evolved to adaptively include what must be tested and how it must be tested. This has varied from one technology to another, from one functional IP / SOC design to another and from one end application to another. These adaptations have also evolved across different ATE (automated test equipment) platforms, since the compelling needs to use low cost test platforms and to not invest in newer platforms very frequently continue to determine which test solutions are affordable.

While it is well-known that we must test for as many defects as possible, test tools must model or approximate defects into likely faults and into measurable errors using existing and sometimes limited precision instruments on the ATE, thereby setting the path to “approximate test”.

In this special issue, we will solicit papers from various academic, research and industry groups on how best to apply “approximate” test methods to meet the objectives listed above. These papers will provide insight and justification into why approximate test is perhaps the best answer to test all functions implemented in silicon, i.e. data and signal manipulation and transmission in analog / mixed signal and digital circuits, under controlled power, external interface driven and application use case conditions.

Topics of Interest

- Use of statistical and machine learning methods to complement normal production tests, and enhance quality and reliability. Challenges in developing accurate predictive models.
 - Use of on-die sensors in test to improve chip internal visibility and test measurement resolution.
 - Design for test (DFT) and built-in self test (BIST) methods to overcome limitations of test solution (instruments and hardware interface).
 - Economics of thorough vs approximate testing. Approximate test methods enabled through design and DFT, test HW external to the DUT (device under test), test flows, and test data analysis.
 - Device trimming and precision versus test time trade-offs. Optimization methods to exploit test tolerance.
 - Timing and delay testing measurement accuracy. Test methods for improvement of screens.
 - I_{DDQ} and leakage testing. Challenges in large and/or high current devices. Techniques for improved defect detection.
- While there is distributed standalone material in the literature on some of these topics, this special issue will serve as a compendium of articles reflecting the state-of-the-art with special focus on how approximate test is being embraced, and what pre-work is needed to make its adoption successful. Directional and survey papers are also welcome.

Submission Guidelines

Prospective authors should follow the submission guidelines for IEEE Design & Test. All manuscripts must be submitted electronically to IEEE Manuscript Central at <https://mc.manuscriptcentral.com/dandt>. Indicate that you are submitting your article to the “Special Issue on Approximate Test”. Manuscripts must not exceed 5,000 words, including figures (with each average-size figure counting as 200 words) and a maximum of 12 references (30 for surveys). This amounts to about 4,000 words of text and a maximum of five small to medium size figures. Accepted articles will be edited for clarity, structure, conciseness, grammar, passive to active voice, logical organization, readability, and adherence to style. Please see IEEE Design & Test Author Information at: <https://ieeecd.org/publication/ieee-design-test-dt/author-info>.

Schedule

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| • Open for submissions | Apr. 17, 2023 | • Revision Submission | Dec. 11, 2023 |
| • Submission deadline | Aug. 07, 2023 | • Final decision | Jan..29, 2024 |
| • Notification First Round | Oct. 23, 2023 | • Tentative publication | Spring 2024 |

Guest Editors

- Rubin Parekhji, Texas Instruments (India).
- Ken Butler, Advantest America, Inc. (USA).

For questions and other information, please contact the guest editors at parekhji@ti.com and ken.butler@advantest.com