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CEDA Currents

IEEE Council on Electronic Design Automation

An Update from the 2008 MEMOCODE HW/SW Co-Design

Contributed by Patrick Schaumont (Virginia Tech), Krste Asanovic (UC Berkeley) and James C. Hoe (Carnegie Mellon Univ.)

The second running of the MEMOCODE HW/SW Co-Design Contest concluded successfully on March 9, 2008. This annual contest was conceived for the MEMOCODE Conference (http://memocode-conference.com) to help highlight the issues distinct to HW/SW co-design and to expand the conference's emphasis on design and practice. On February 8, a "secret" design problem (involving AES and sorting) was revealed on the contest website, giving the contestants one month to produce working HW/SW co-designed solutions that compete in performance and in the elegance of design. By the conclusion of the contest, eleven entries from around the world (including US, Europe and Asia) were submitted out of the twenty-seven teams that started. The final design entries are currently being evaluated by a panel of judges to determine the winners for the contest. The results will be formally announced at the MEMOCODE 2008 Conference, June 5-7, Anaheim, CA (co-located with DAC).

This year's contest will award two $1000 cash prizes in the categories of The Highest Performance Design and The Most Efficient Design. In addition, Xilinx is sponsoring a special $1000 cash prize for the best entry employing a high-level design methodology. This year's contest is organized by Patrick Schaumont (Virginia Tech), Krste Asanovic (UC Berkeley) and James C. Hoe (Carnegie Mellon University). The panel of judges comprises the three contest organizers, Kees Vissers (Xilinx) and Satrajit Chatterjee (Intel). This year's contest is sponsored by Nokia, Xilinx, Bluespec and IEEE CEDA. In http://rijndael.ece.vt.edu/memocontest08 you can see a description of the design problem and the contest rules.

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IEEE Annual Honors Ceremony

The annual Honors Ceremony, considered to be IEEE's most prestigious event, recognizes exceptional contributions that have made a lasting impact on technology, society and the engineering profession. The program honors achievements in industry, research, education and service. There will be 17 Institute-level award recipients recognized at the 2008 IEEE Honors Ceremony.

The event will be hosted by the 2008 IEEE President and CEO, Lewis Terman. The theme for the IEEE Honors Ceremony will be "Innovating to Meet the World's Challenges."

This year's IEEE Honors Ceremony will be held on Saturday, 20 September 2008, in conjunction with IEEE Sections Congress at the Quebec City Convention Center, Quebec, Canada. The ceremony is planned to start at 6:00pm that evening, with a dinner and afterglow reception immediately following the conclusion of the ceremony.

All those attending Sections Congress are invited to the IEEE Honors Ceremony, dinner and afterglow reception.

For further information, please visit the "Awards News" in the IEEE website.

Networks-on-Chips and EDA Tools to Improve Energy-Efficiency of MPSoC Designs

Reported by Prof. Srinivasan Murali (EPFL, Switzerland)

Many MPSoCs are used in many devices, where a low energy operation of the system is critical. As technology avances, wire scaling is not on par with transistor scaling. This, coupled with the fact that the number of communicating components in the chip and their speed of operation is increasing, has lead to the scenario where the communication between the cores is a major bottleneck for system performance and energy consumption. With architectures being more interconnect dominated, achieving an energy efficient on-chip interconnect architecture, tailored to the needs of the applications running on the chip is an important challenge faced by the designers.

In recent years, researchers have been addressing this challenge in two ways: by developing methods and CAD tools to achieve an energy-efficient design and by developing scalable micro-network based architectures

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(NoCs). CAD tools allow an exploration of the interconnect design space early in the design cycle and automate the building of efficient application-specific interconnect architectures. The NoC paradigm results in structured, modular interconnect design with improved performance and energy efficiency.

The main goal is to allow designers to explore trade-offs in interconnect design, e.g. between bandwidth, power, reliability, area cost. State-of-the-art methods do exist to solve some of the most important and time-intensive problems encountered during interconnect design, such as interconnect topology synthesis, core mapping, crossbar sizing, route generation, resource reservation, RTL code and layout generation. Application specific interconnect optimization can lead very significant improvements in all relevant cost metrics. Factors of 2 to 5 improvements are not uncommon, and become even more significant with technology and architectural complexity scaling. Design automation support is essential to guarantee that these custom-fit solutions can be readily deployed, tested and verified. Even though the state of maturity of these tools is not perfect, results are promising, and automated interconnect design is poised to become an essential component in energy aware SoC design and validation flows.

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IEEE memberNet Online Directory

The IEEE launched on March its online member directory which connects its 375,000 members worldwide. Access to IEEE memberNet is an exclusive benefit of IEEE membership, available at no additional cost to IEEE members.

"IEEE memberNet will fundamentally transform peer-to-peer networking within the IEEE membership," says Joseph Lillie, Vice President, IEEE Member and Geographic Activities. "This is the first step in a series of next-generation capabilities to enable our members to connect and collaborate virtually. In this way, members can discover other members with similar technical and engineering interests – regardless of geography."

IEEE memberNet is driven by member participation, according to Lillie. "The full benefit is dependent upon the scope and degree of our members' opt-in participation."

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While the basic member profile in memberNet contains every member's name and membership grade, each member can indicate by check mark what additional information they would like to also have appear. These may include technical interests, local Section, or IEEE Society affiliation. "The check mark approach saves time for our members," said Lillie, "as they do not need to re-key information to create their memberNet profiles."

For more information, please contact Brian Pratz at b.pratz@ieee.org.

IEEE Electron Devices Society Seeks Nominations for Ph.D. Student Fellowship Program

The IEEE Electron Devices Society (EDS) invites the submission of nominations for the 2008 Ph.D. Student Fellowship Program. The award is presented annually to promote, recognize and support Ph.D. level study and research within the EDS' fields of interest. Candidate must: be an IEEE EDS student member at the time of nomination; be pursuing a doctorate degree within the EDS field of interest on a full-time basis; and continue his/her studies at the current institution with the same faculty advisor for twelve months after receipt of award. Sponsor must be an IEEE EDS member. Previous award winners are ineligible. At least one fellowship is awarded to a student in each of the following geographical regions every year; Americas, Europe/Middle East/Africa and Asia & Pacific. The award is a check for US$7,000 and a plaque presented at the IEEE International Electron Devices Meeting (IEDM). The deadline is 15 May 2008.

For further information, please visit the "Education Section" in the IEEE website.

Upcoming Conferences */ Bill Joyner, william.joyner@src.org*	
ESWEEK	Atlanta (USA), Oct. 19-24, 2008
DAC	Anaheim (USA), June 8-13, 2008
ICCAD	San Jose (USA), Nov. 10-13, 2008
FMCAD	Portland (USA), November, 2008
Nano-Net	Boston (USA), Sept. 15-17, 2008
MEMOCODE	Nice (France), May 30-June 1, 2008
MPSoC	Aachen (Germany), June 23-27, 2008
PATMOS	Lisbon (Portugal), Sept. 10-12, 2008
VLSI-SOC	Rhodes (Greece), Oct. 13-15, 2008
GLSVLSI	Orlando (USA), May 4-6, 2008