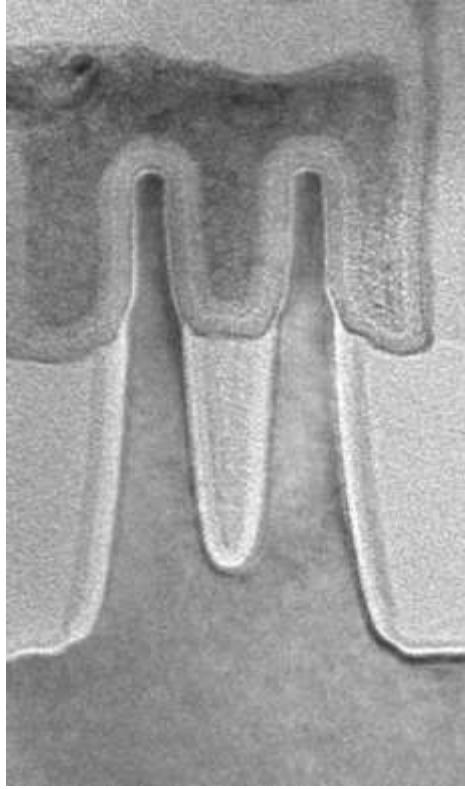


Process Technology Variation

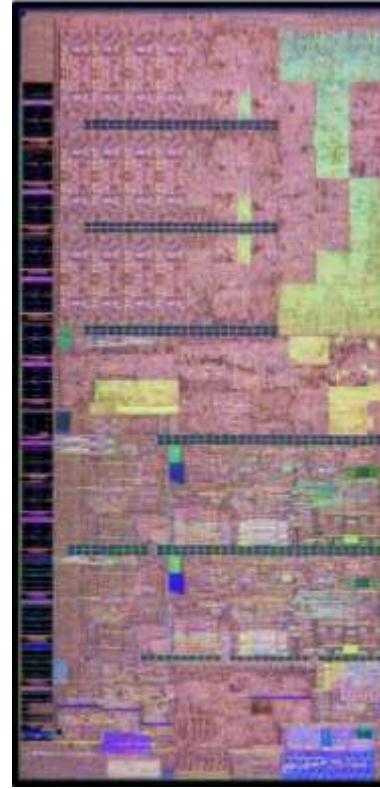
Martin D. Giles
Intel Corporation

ICCAD TCAD to EDA Workshop
November 2, 2014

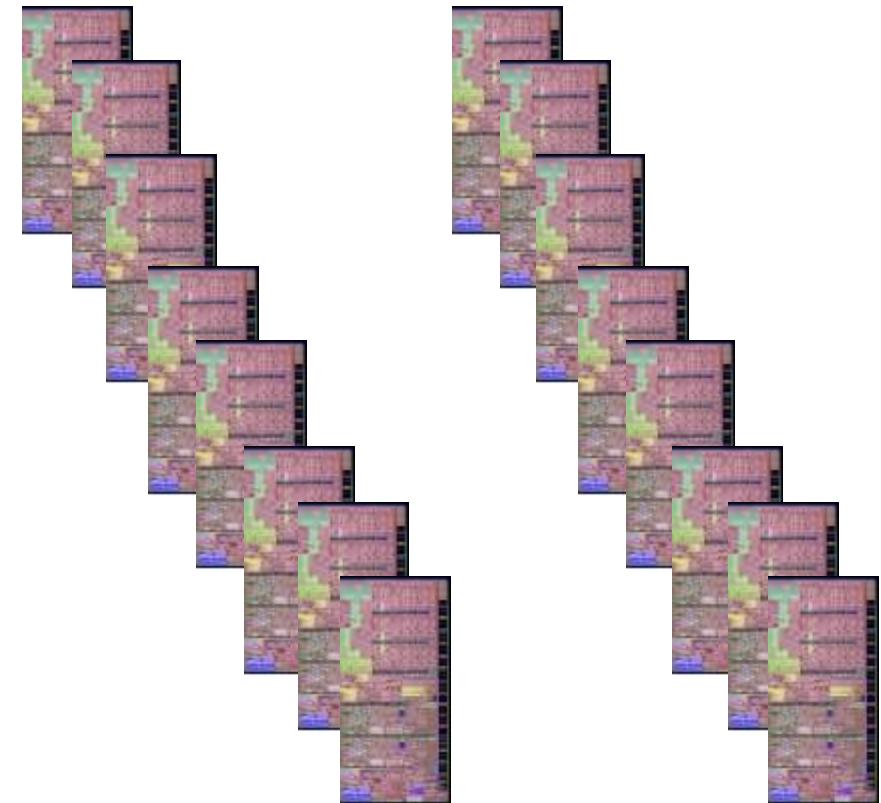
The Variation Challenge



1 => many transistors
Random



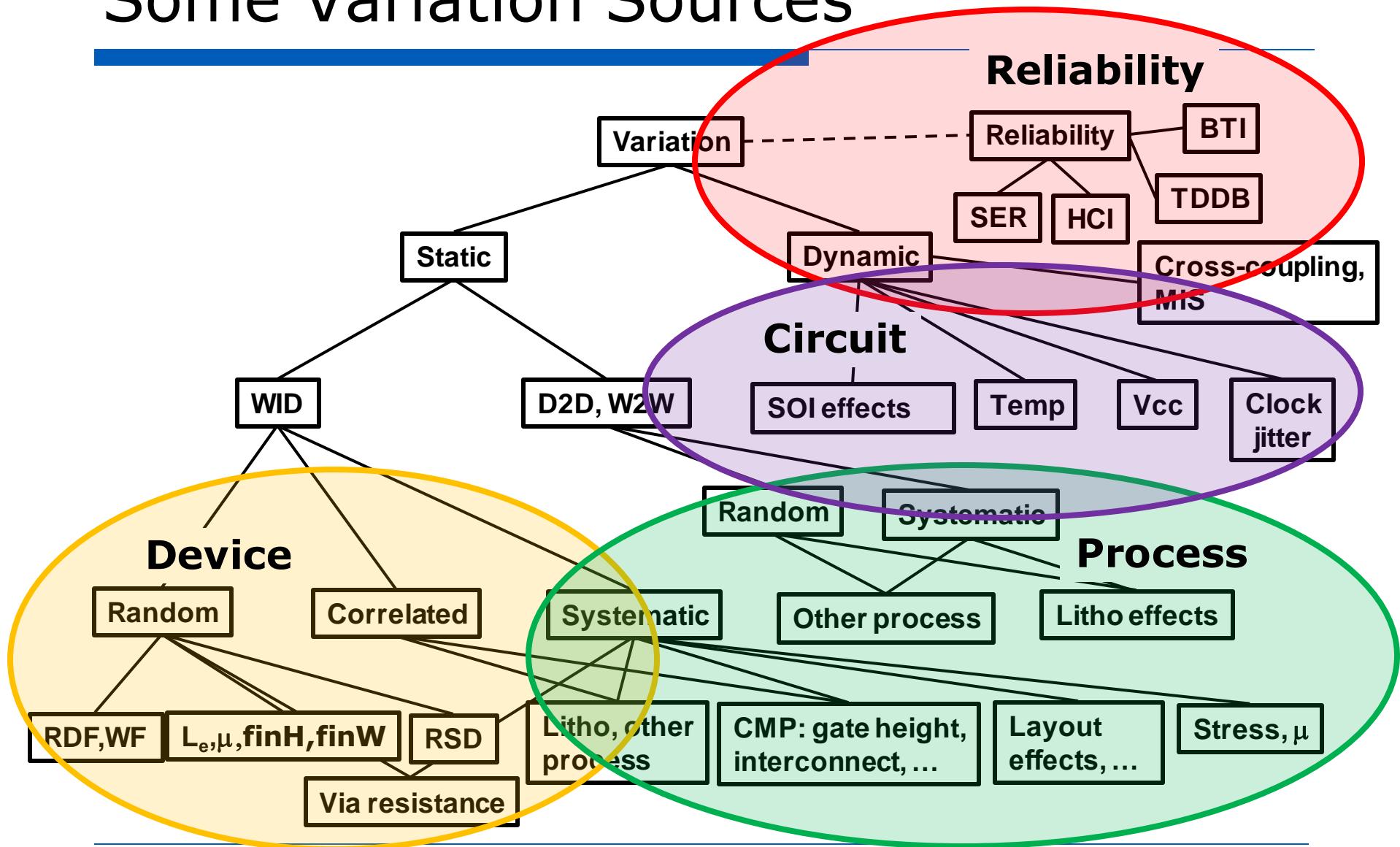
1 => many die
Systematic



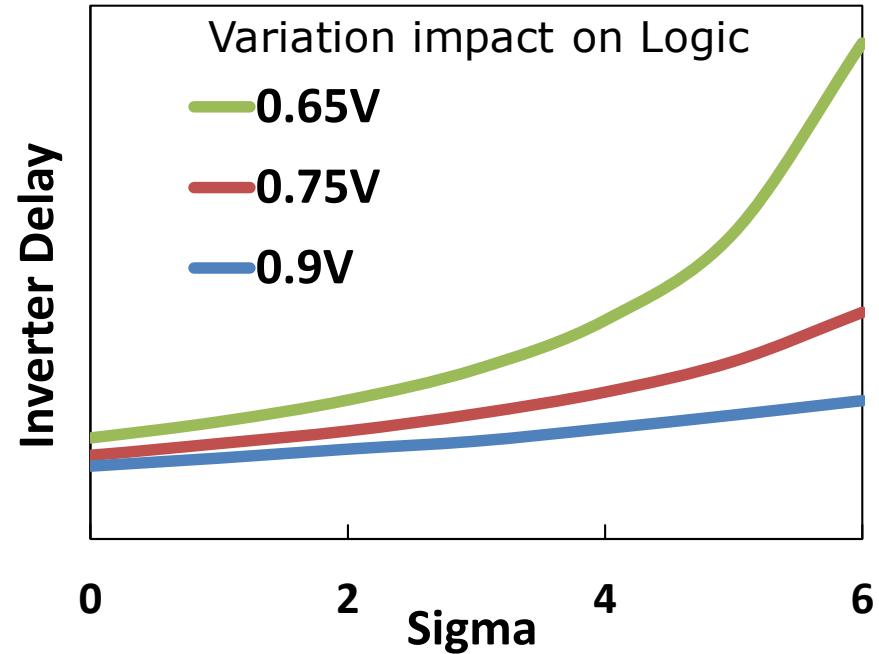
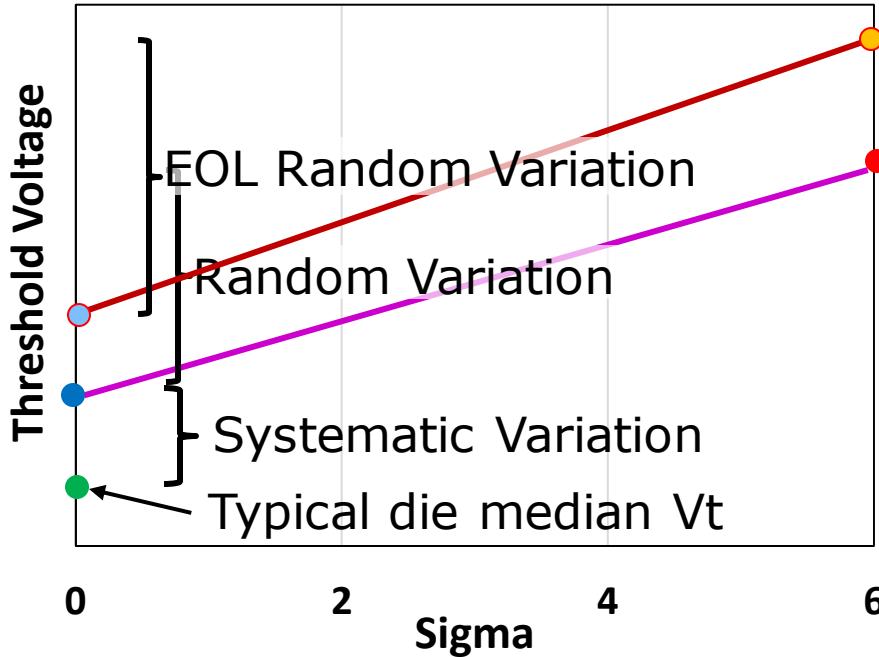
Time-0 => EOL
Reliability

Intel 14nm Tri-Gate Technology

Some Variation Sources



Vt Variation Dominates at Low Vcc



- Vt variation includes systematic and random effects
- Aging effects lead to increased median Vt and variation at EOL
- Delay is highly non-linear at high Sigma and low Vcc

Modeling Variation

Modeling Device Variation

Source:
process variation

Consequence:
structure variation

Effect:
electrical variation

Flow patterns
Shot noise
Thermal gradients
Quantization
Random processes

Charge distribution
Gate shape
Oxide thickness
Contact opening
Grain structure

Vt shift
Lower current
Higher leakage
Higher capacitance

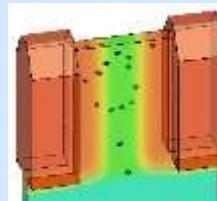
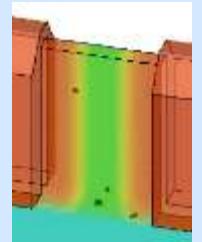
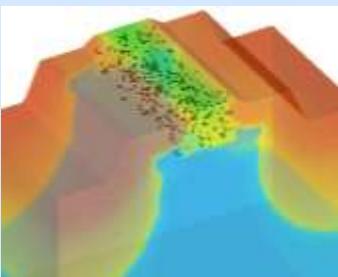


Experimental Data

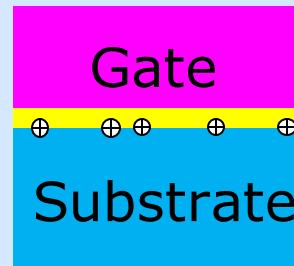
- 1) Modeling the distribution of physical structure variation
- 2) Modeling the electrical response to a physical variation

Random Variation

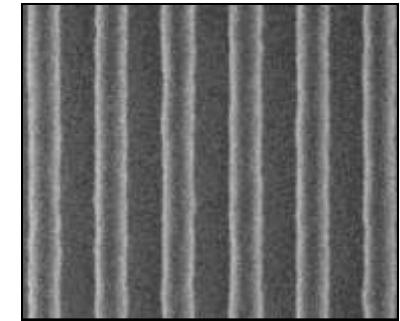
Doping



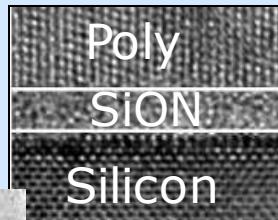
Interface Charge



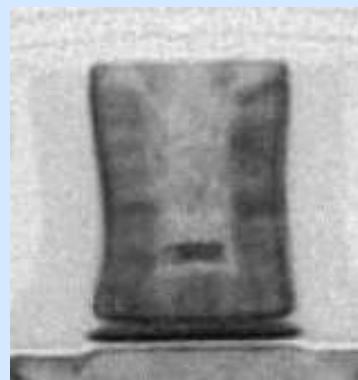
Line Edge Roughness



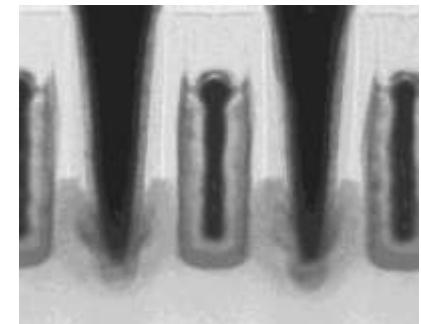
Dielectric Thickness



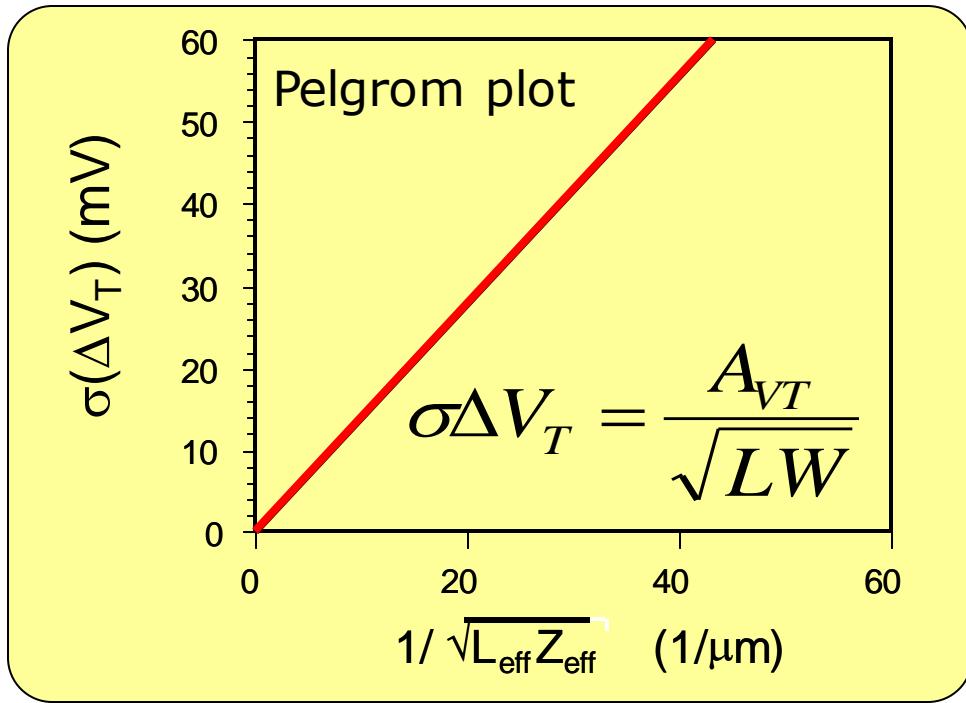
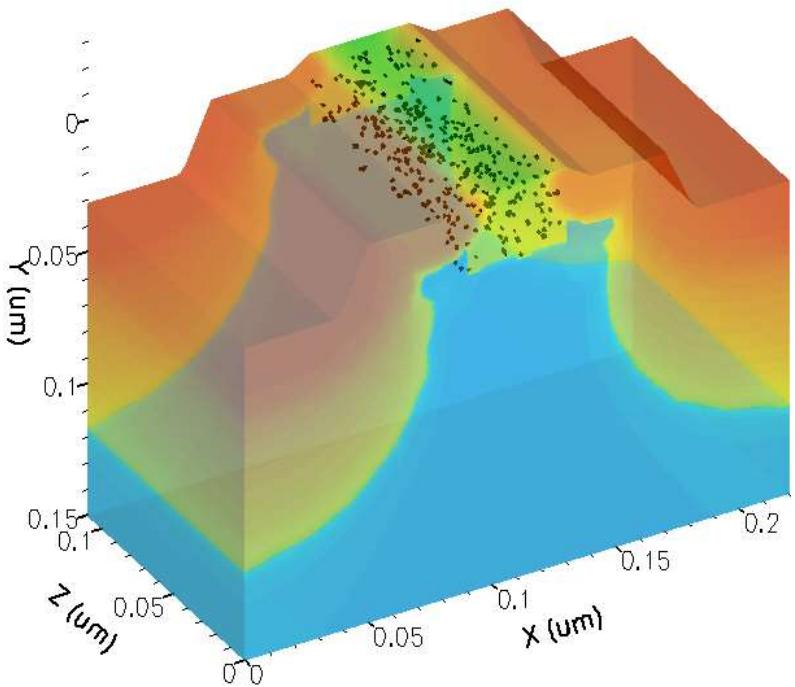
Metal Gate



Contact Resistance



Classic Random Dopant Fluctuation

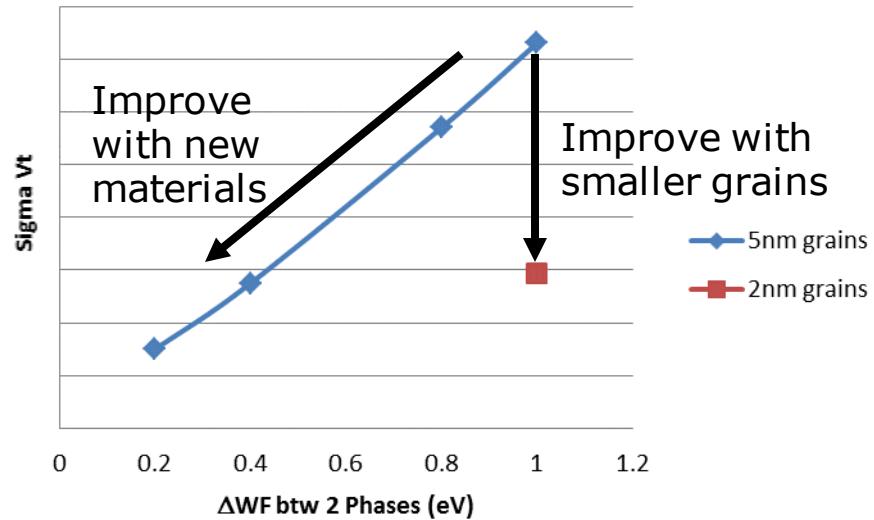
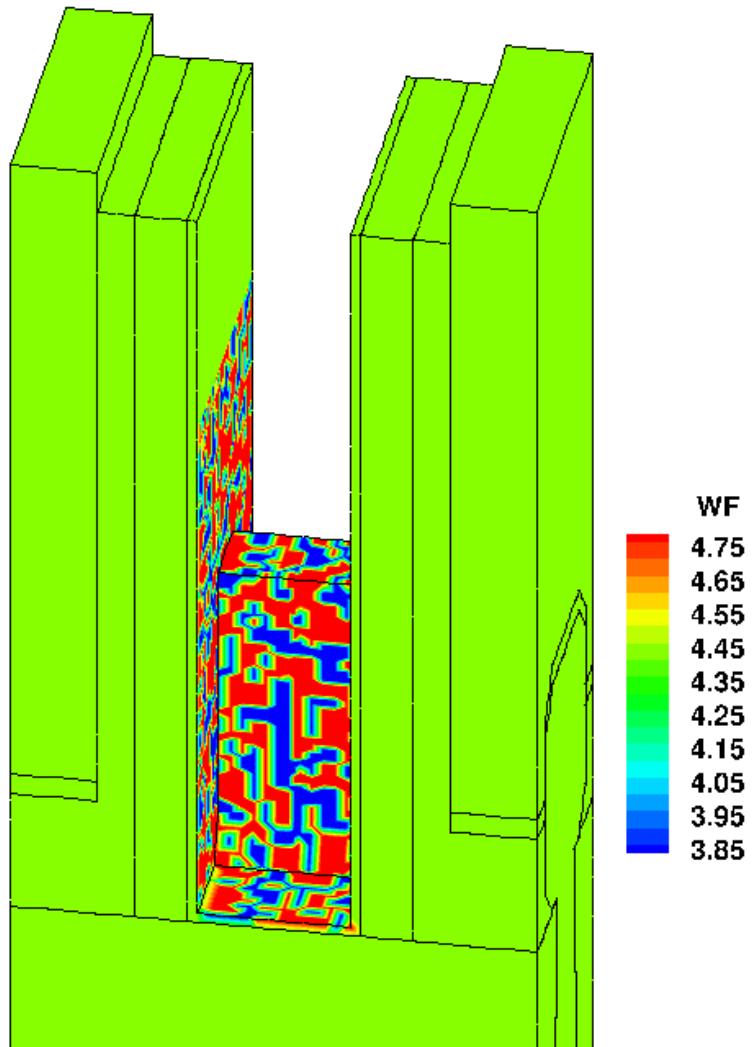


RDF in planar bulk MOS is frequently described by

$$\sigma V_T = \left(\frac{\sqrt[4]{4q^3 \epsilon_{si} \phi_B}}{2} \right) \cdot \frac{T_{ox}}{\epsilon_{ox}} \cdot \left(\frac{\sqrt[4]{N}}{\sqrt{L_{\text{eff}} \cdot Z_{\text{eff}}}} \right) = \frac{1}{\sqrt{2}} \left(\frac{A_{VT}}{\sqrt{L_{\text{eff}} \cdot Z_{\text{eff}}}} \right)$$

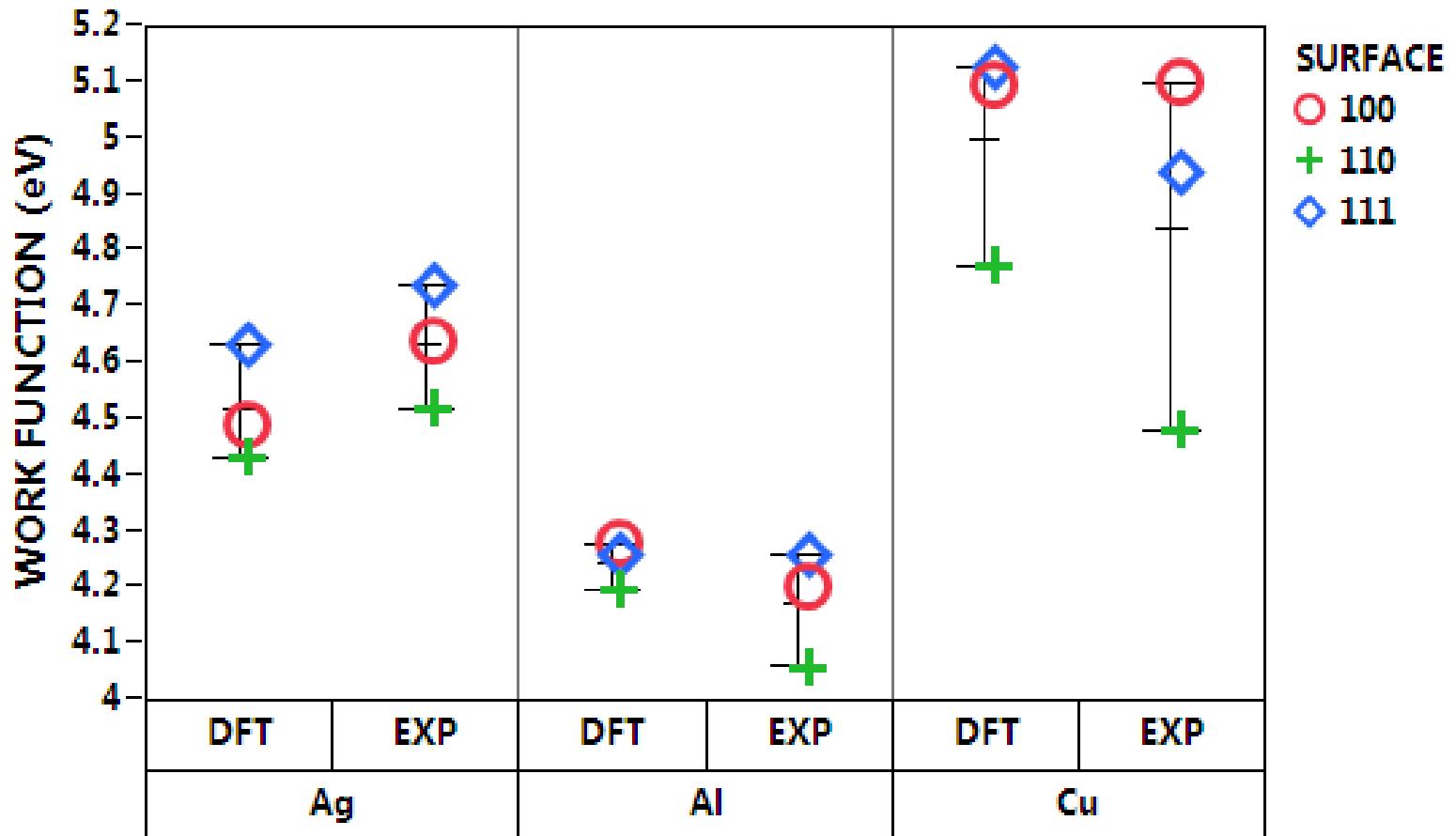
P. Stolk, IEEE Trans. Elec. Dev. 1988

Metal Gate Grain Variation



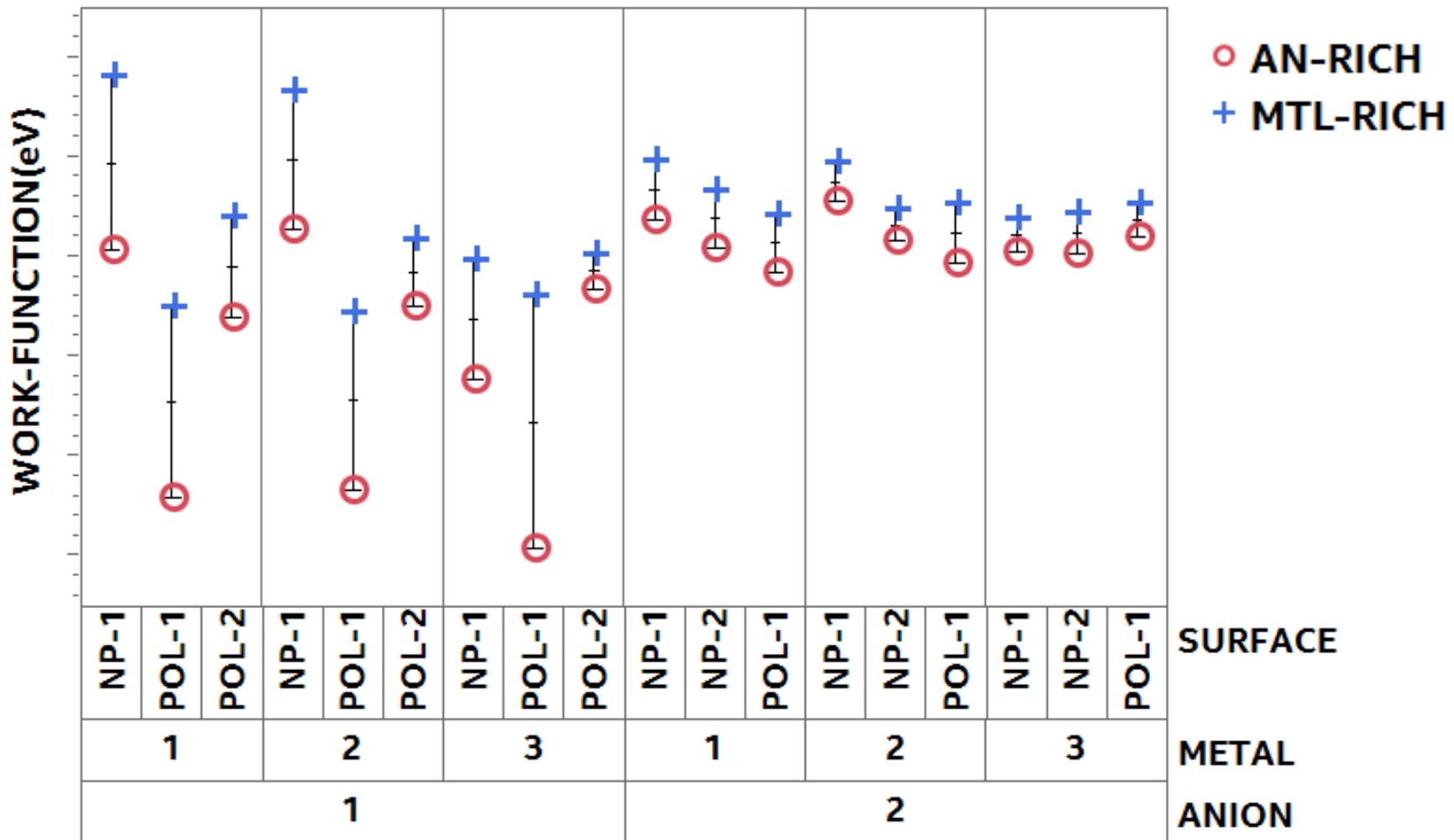
- Metal grain workfunction depends on the orientation
- Causes random V_t variation
- Improve with
 - Smaller grain size
 - New materials with less WF dependence on orientation

Work function: Bulk metals

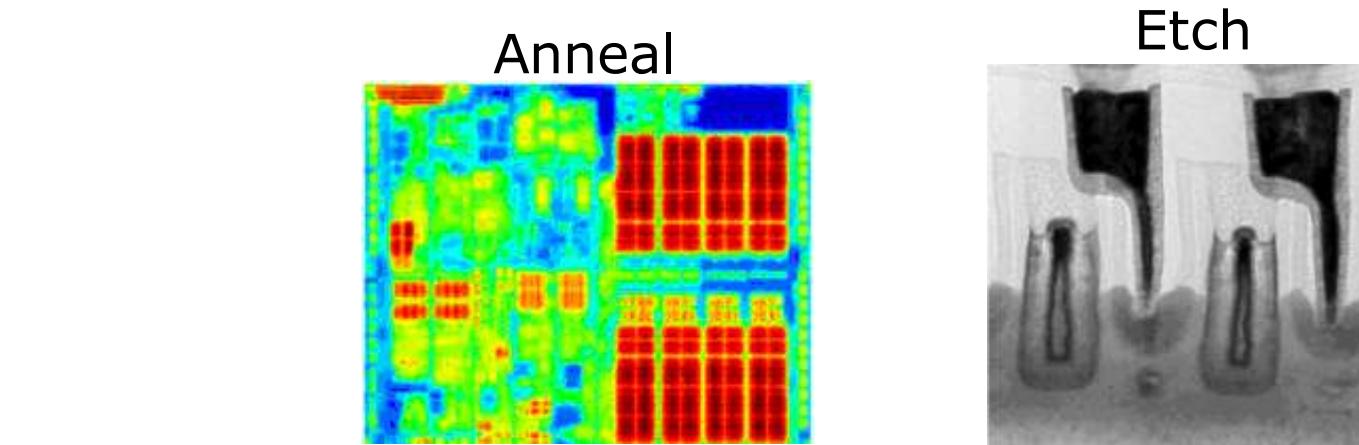
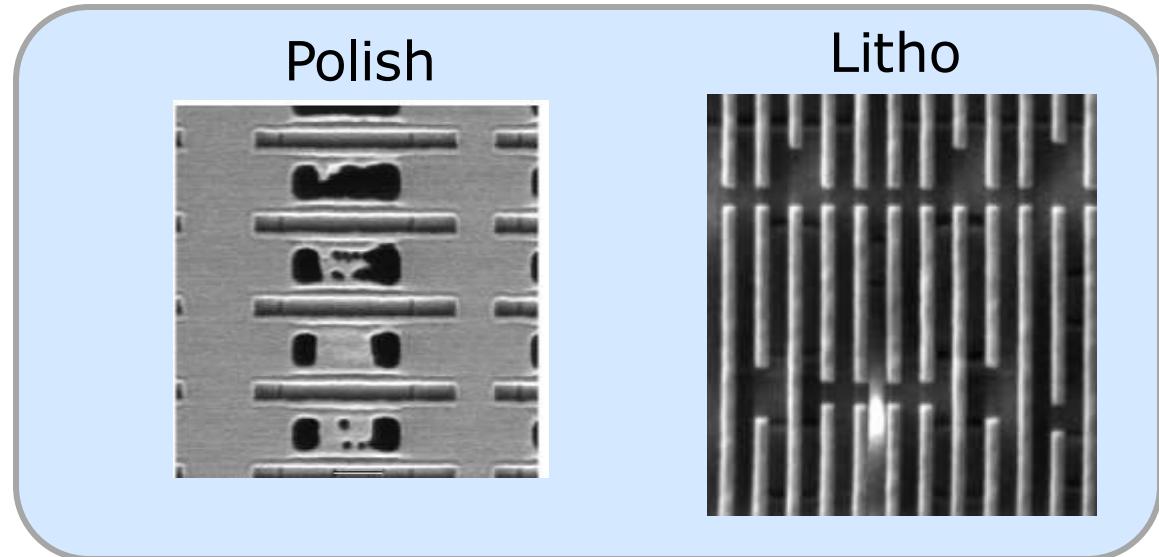
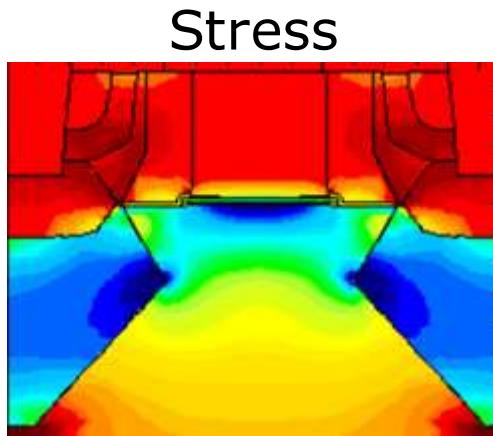


- DFT results are within 0.2-0.3eV of experiment

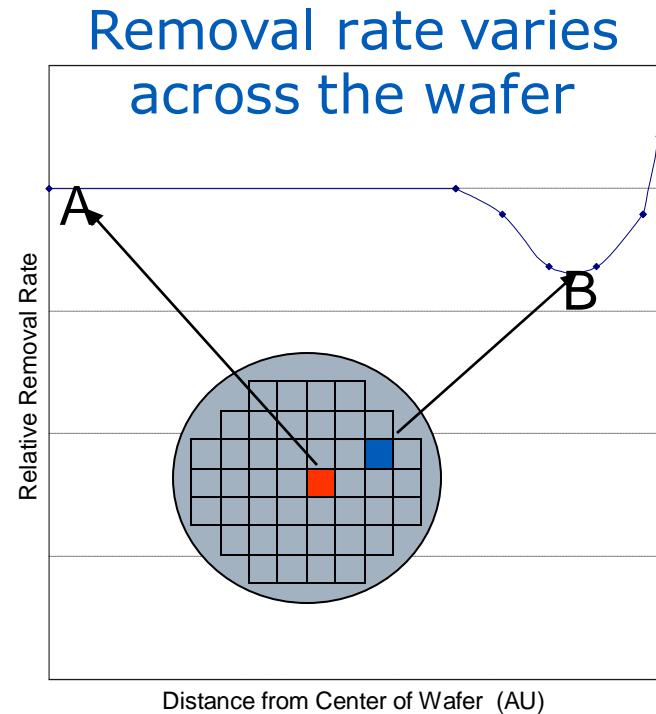
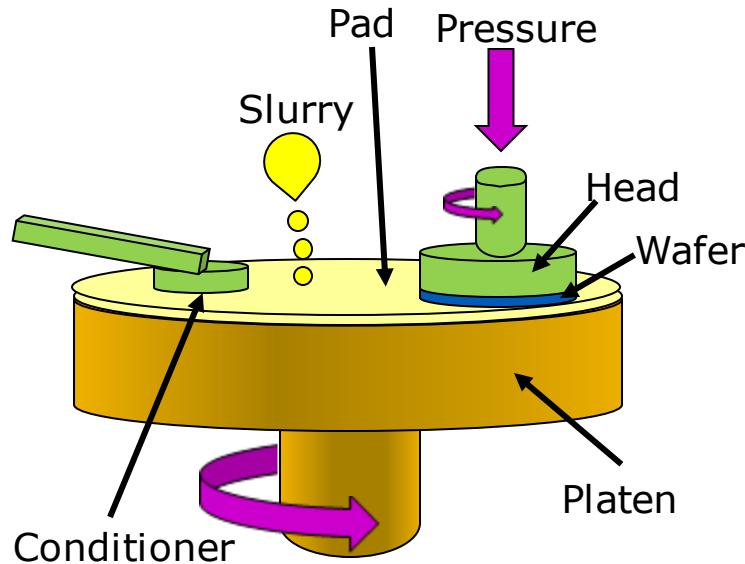
Work function: Compounds Stoichiometry Influences Workfunction



Systematic Variation

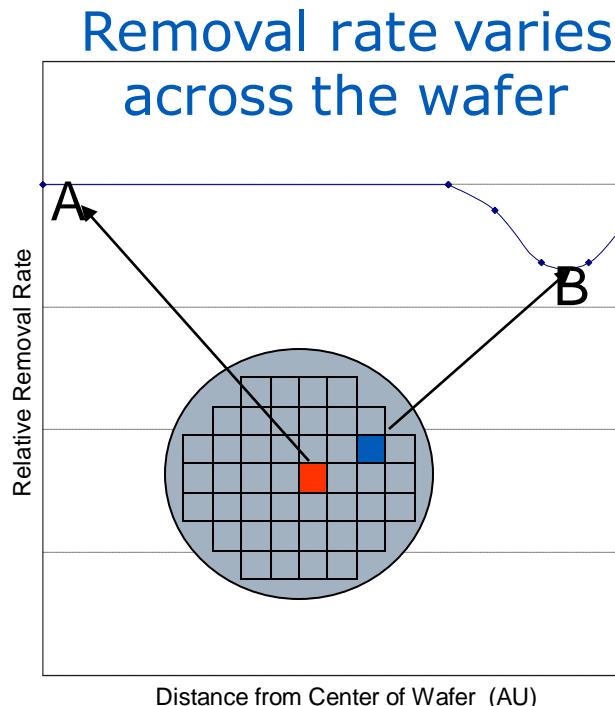


Chemical-Mechanical Polishing

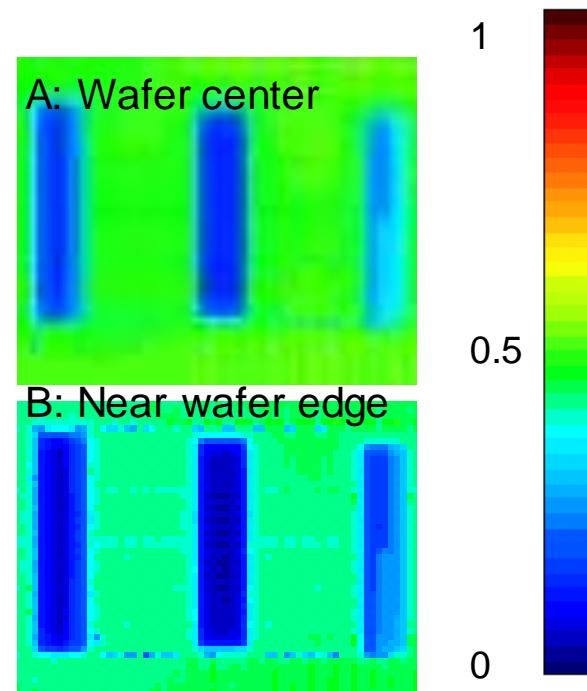


- Material removal rate can vary across the wafer due to
 - Non-uniform pressure distribution
(zone pressure, retainer ring, pad properties)
 - Non-uniform slurry distribution

CMP: Wafer-scale to Within-Die Variation

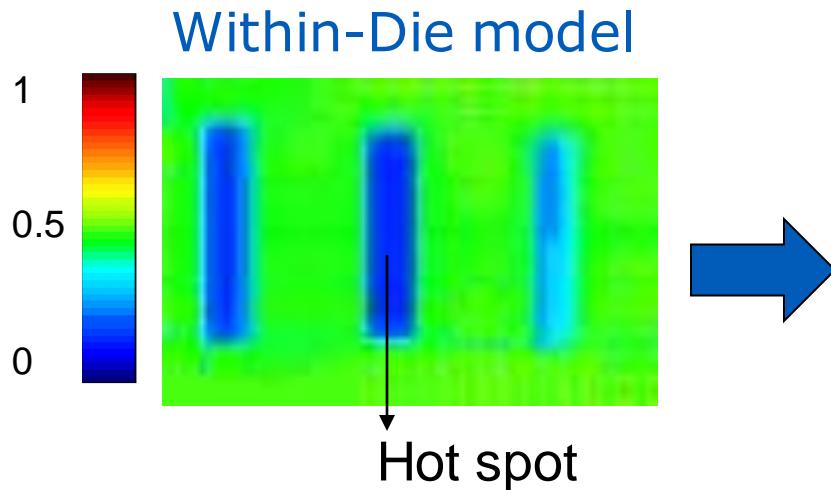


Simulated thickness distribution over proprietary test structure

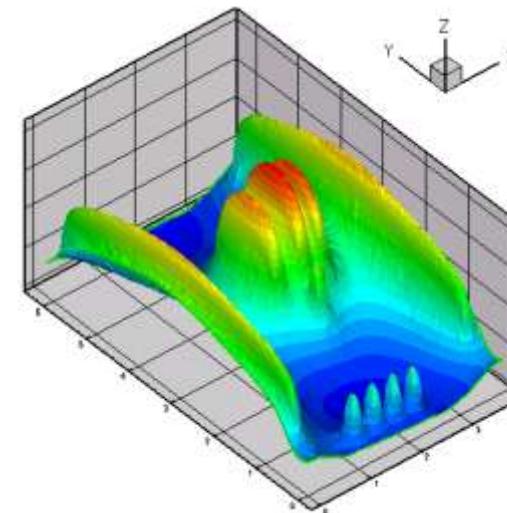


- WID variation is impacted by WIW distribution
 - Structures may respond differently with different WIW variation

CMP: Within-Die to Feature Scale Variation

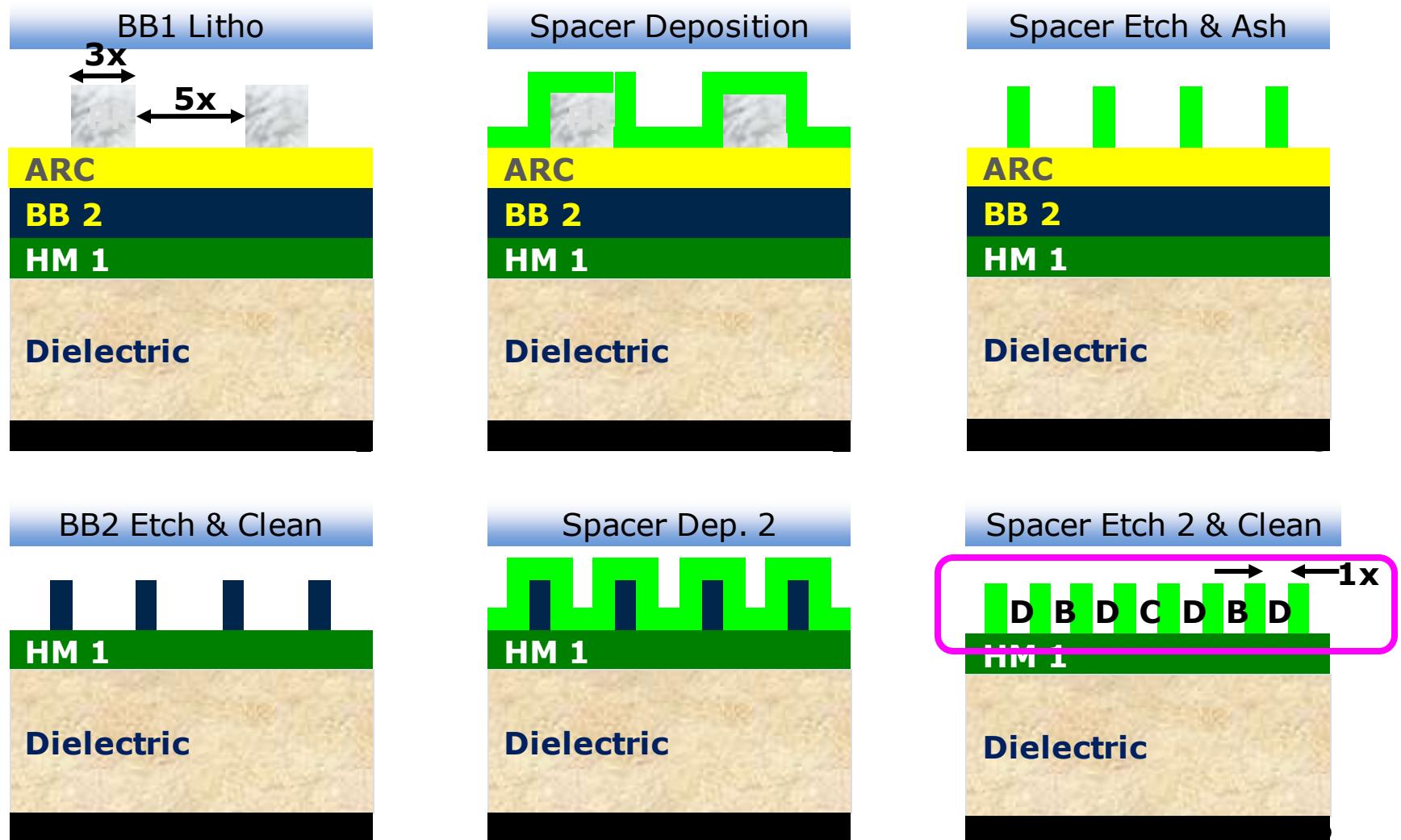


Feature scale CMP simulation
for realistic layout (STI CMP)

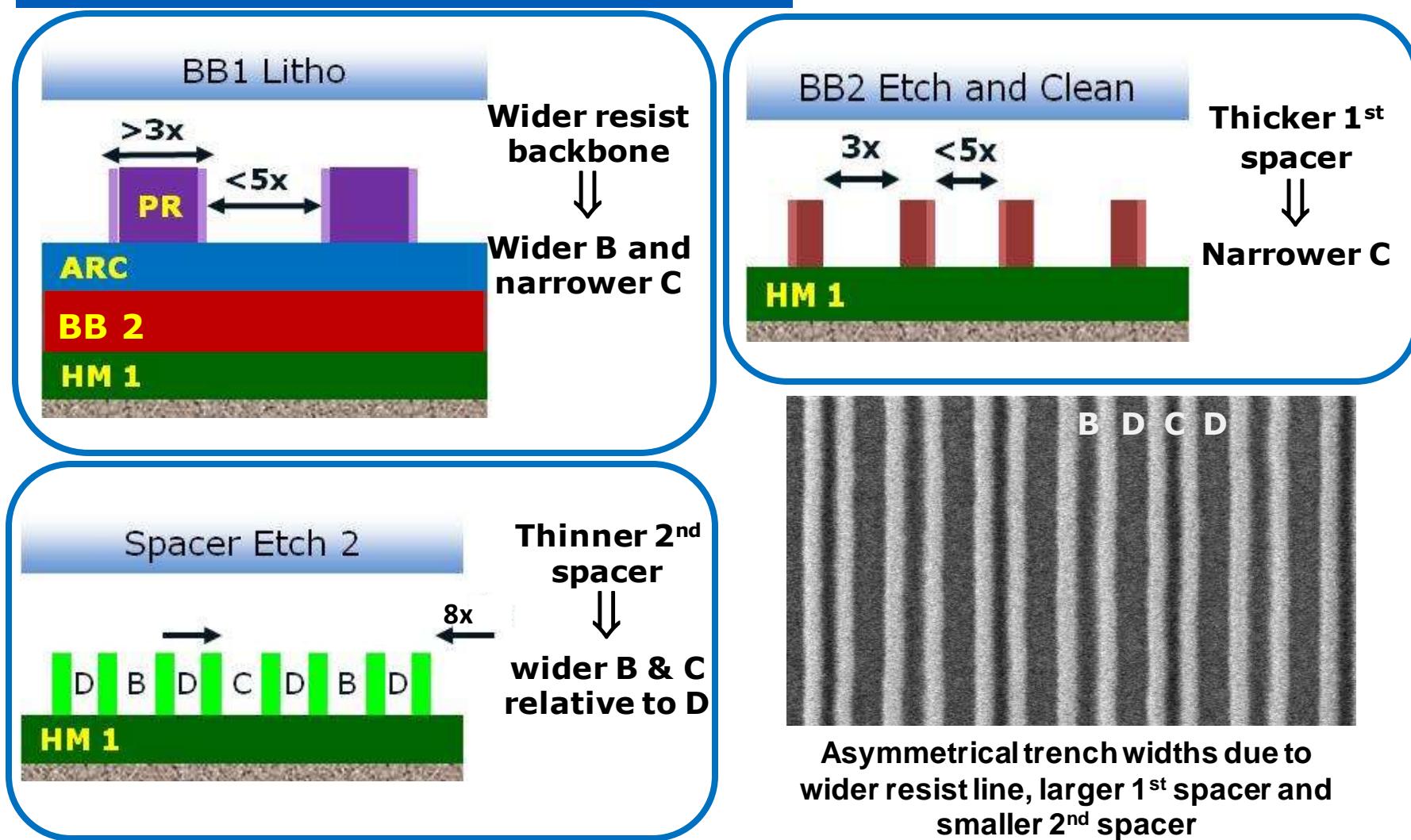


- Hierarchical Modeling Approach
 - WIW model of material removal rate
 - WID model to identify “hot spots”
 - Feature scale simulations for selected hot spots

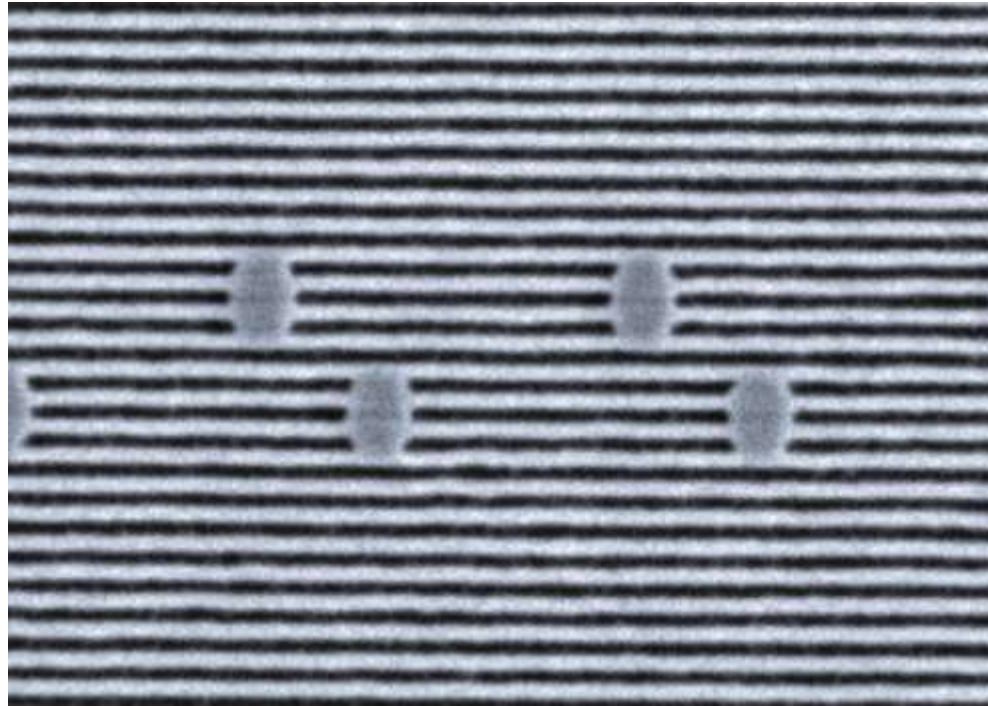
Spacer-Based Pitch Quartering Flow



Quad Patterning Variation



Quad Patterning 34nm Metal Pitch

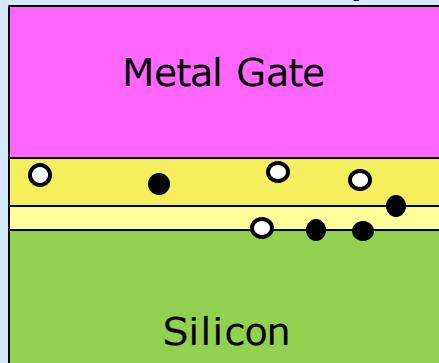


M. Van Veenhuizen et al, IITC 2012

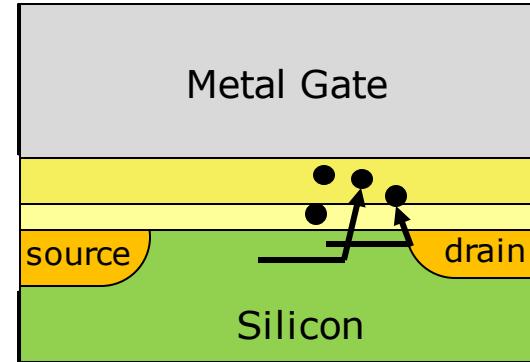
- Optimized process shows good uniformity

Reliability Degradation Mechanisms

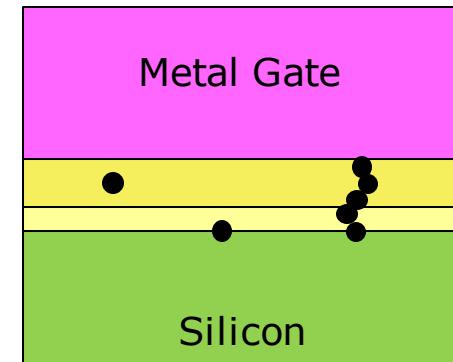
Bias Temperature Instability



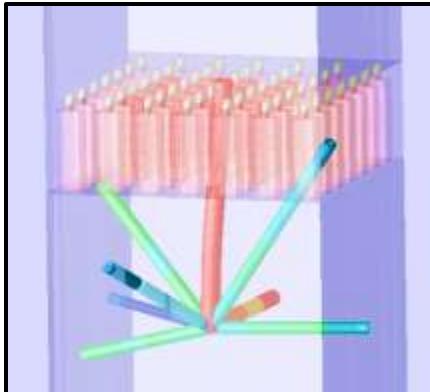
Hot Carrier Injection



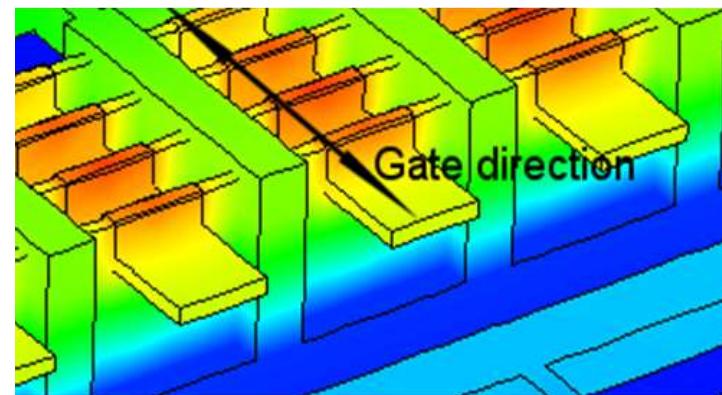
Time-dependent Dielectric Breakdown



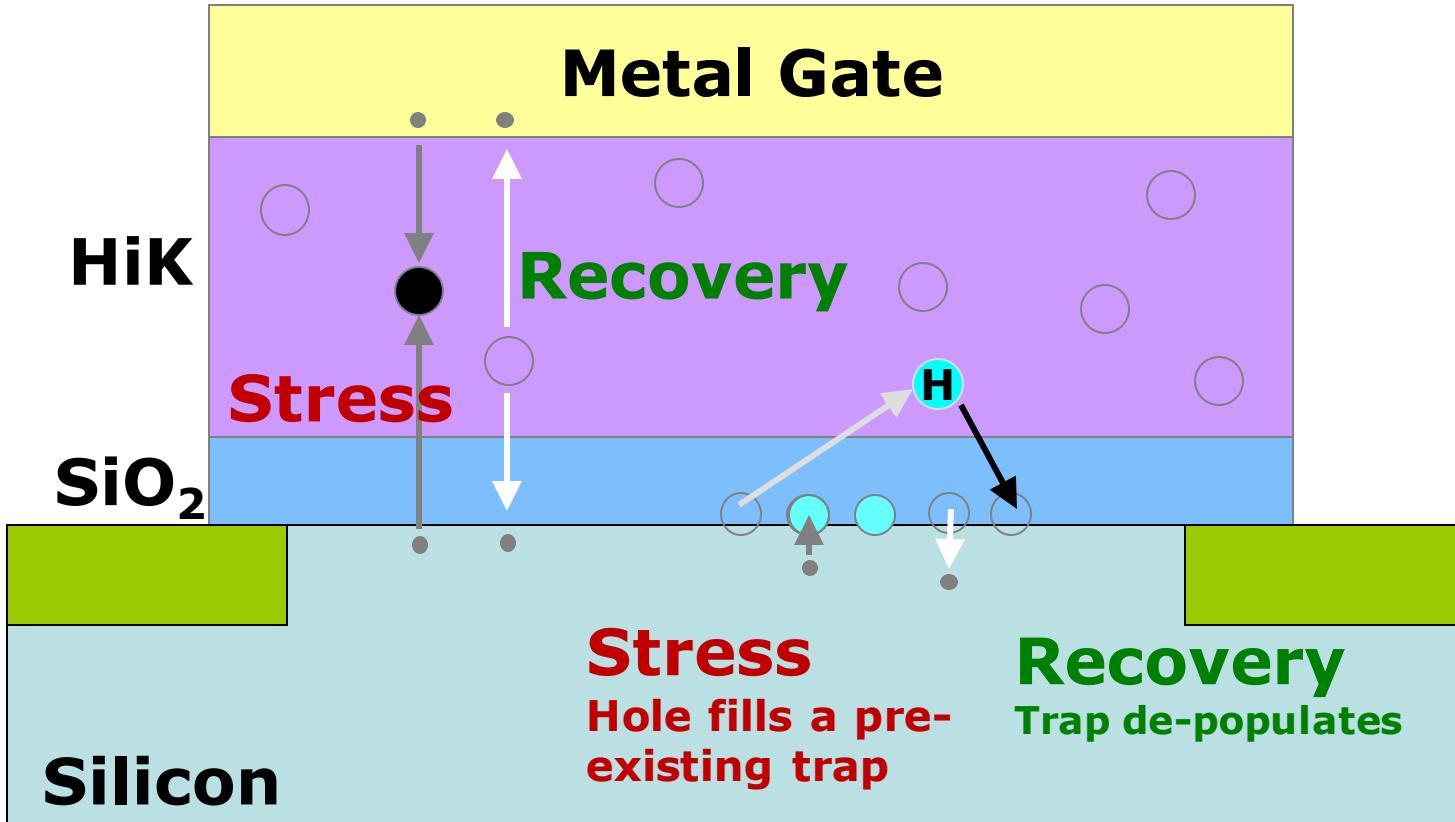
Soft Error



Self-Heat



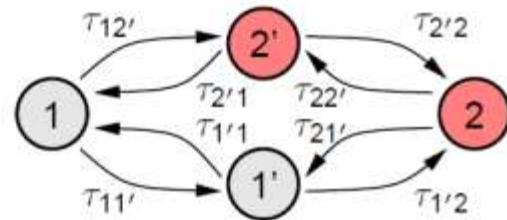
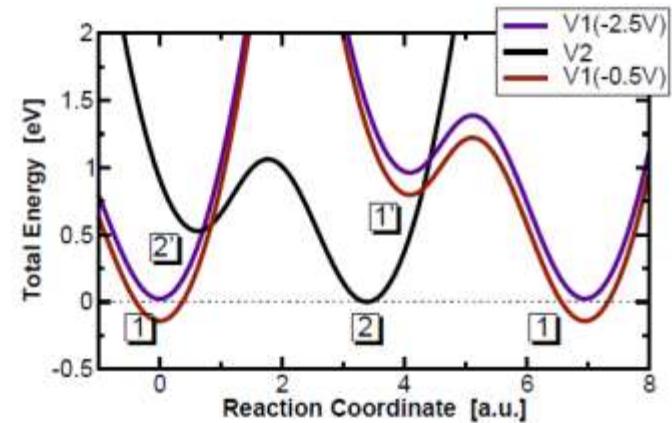
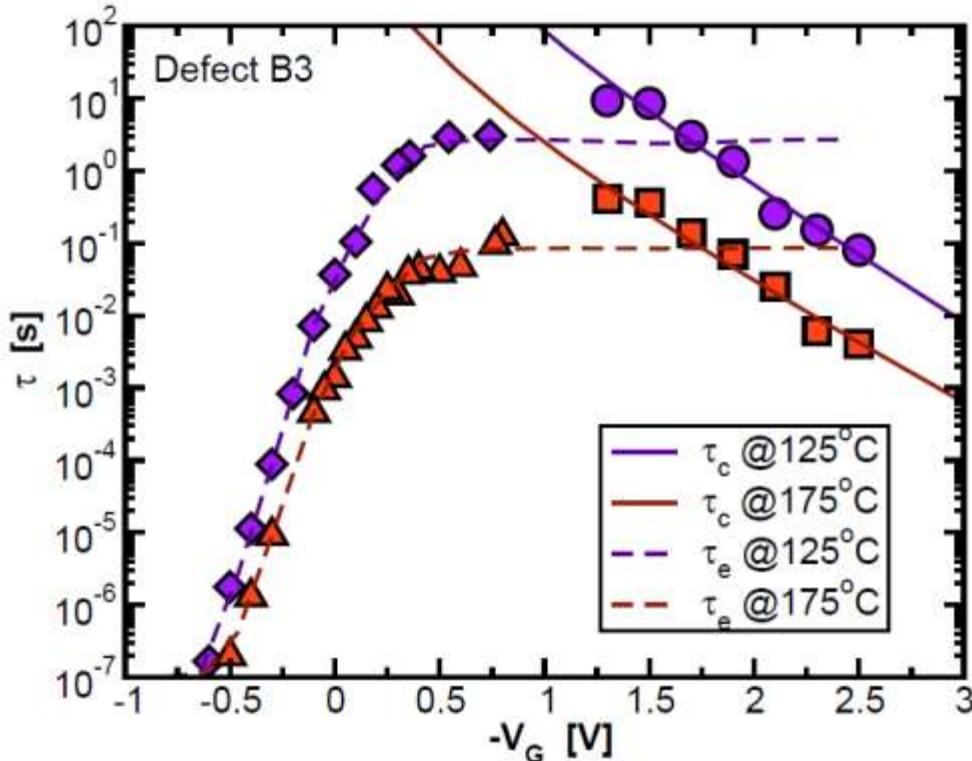
BTI Charge Trapping Picture



- ❑ During stress, traps can be created and existing traps can be filled
- ❑ Recovery is observed when a charged trap depopulates to become neutral
- ❑ Intel data suggests pre-existing traps dominate over a Hydrogen mechanism

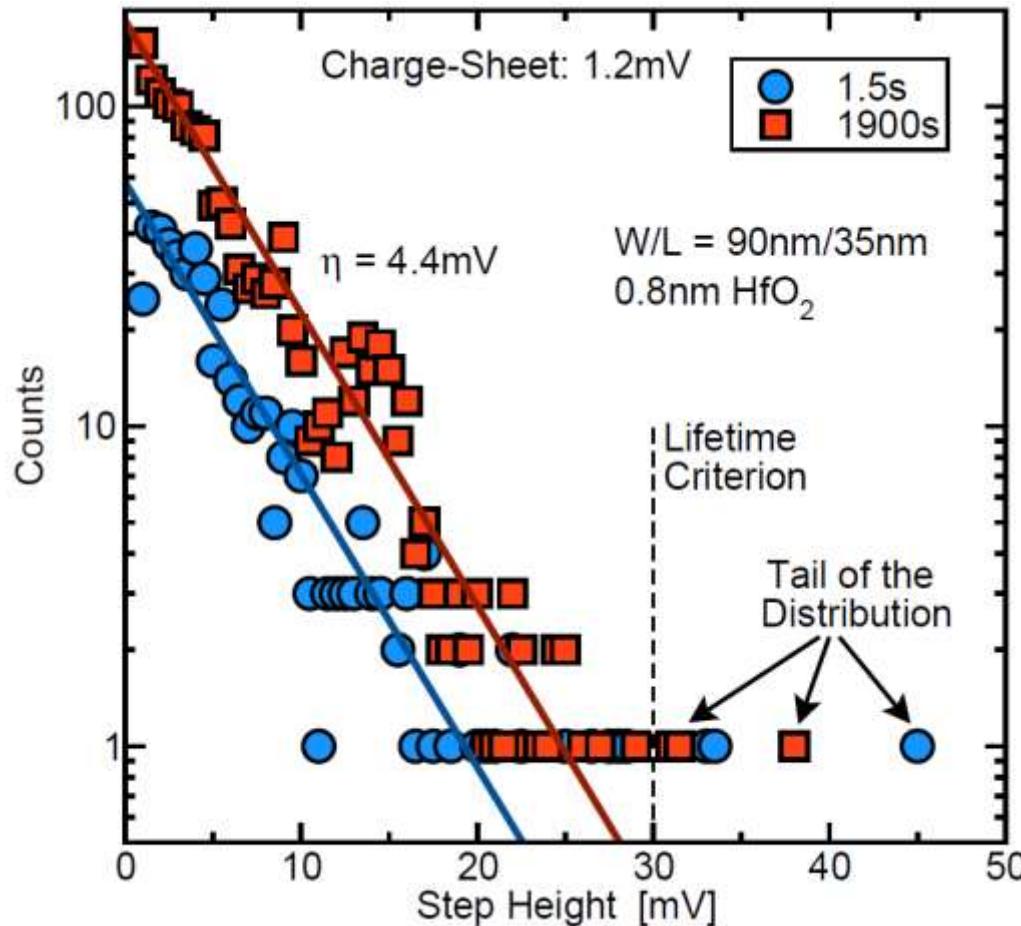
BTI Single Defect Modeling

- Example data from a switching trap with 4 states
- Strongly bias-dependent τ_e

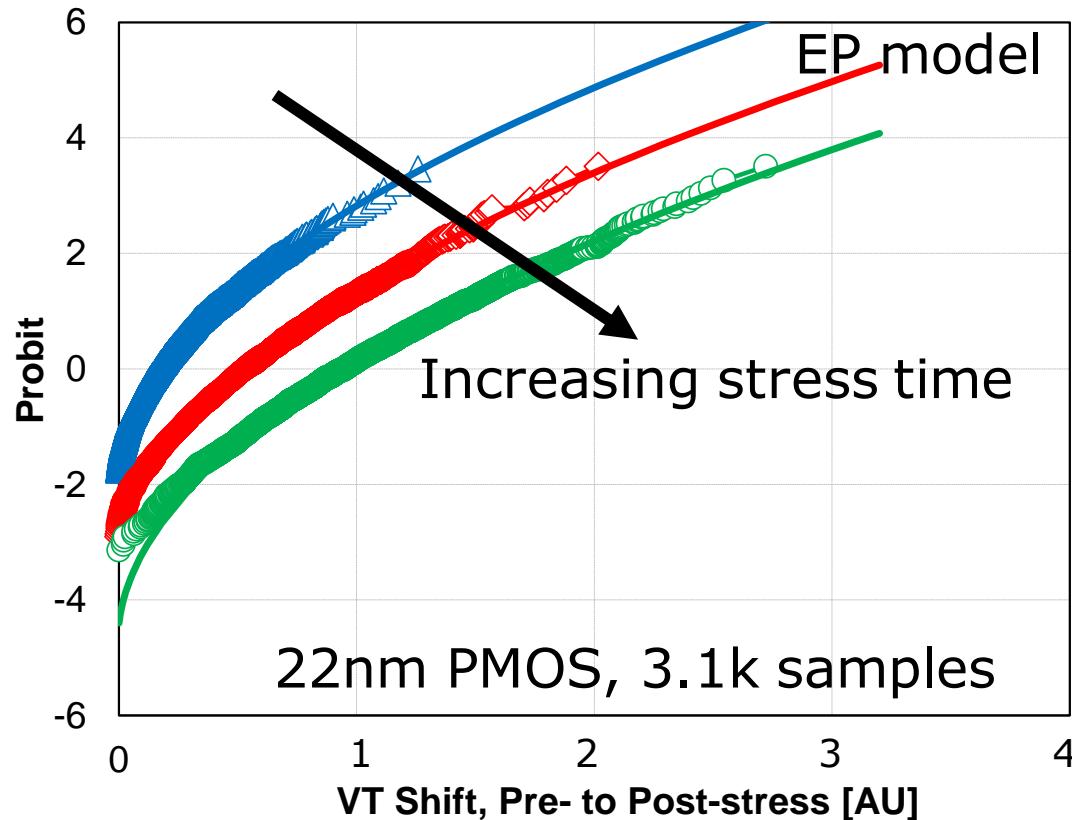


Voltage Step Height Distribution

- RTN/BTI step-heights are exponentially distributed



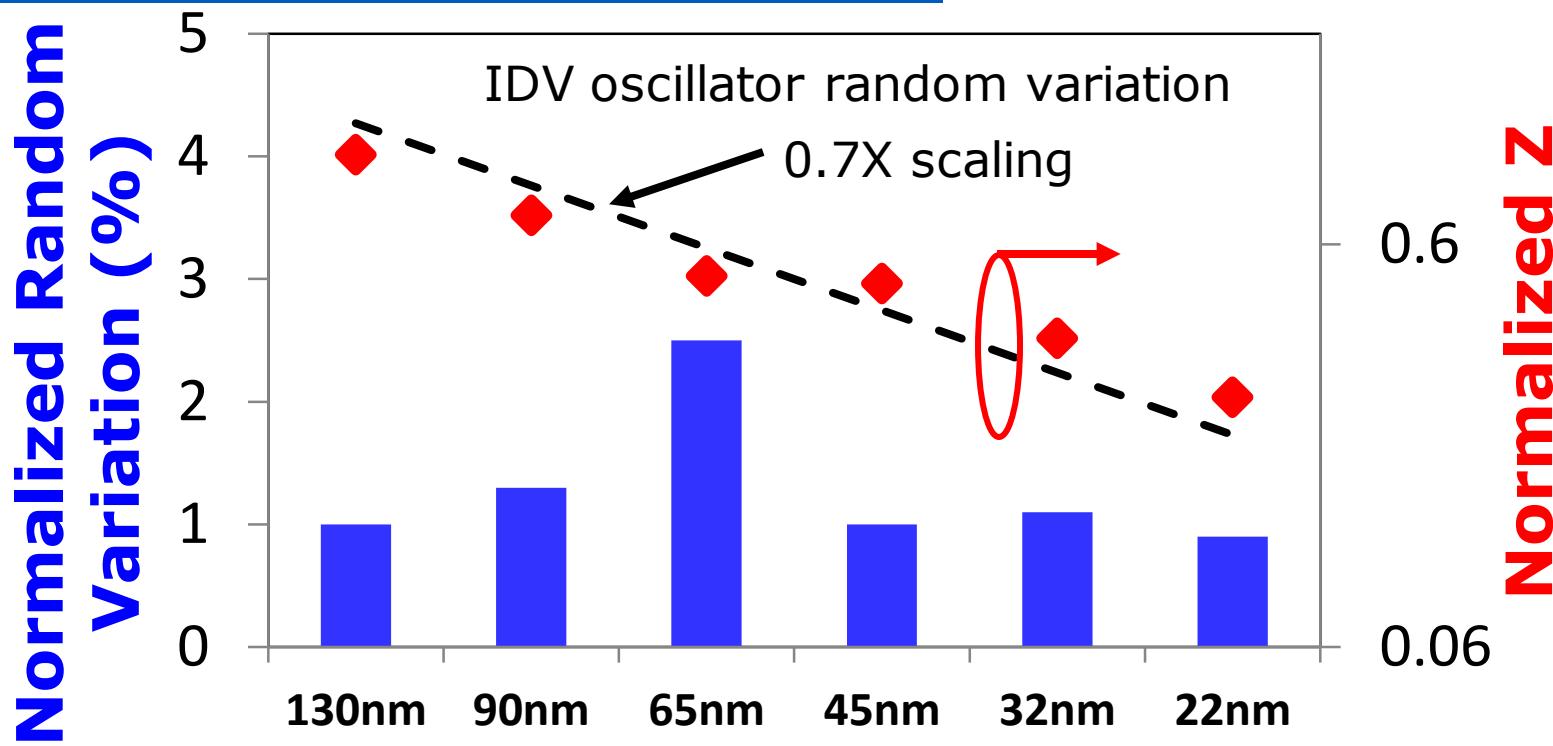
BTI and Vt Variation



- BTI degradation also increases Vt variation
- BTI Vt shift is well described by Exponential Poisson model

Closing Thoughts

Technology Trend



Overcome the variation challenge through continuous technology improvement:

Process + Device + Circuit + Reliability

Modeling Device Variation

Source:

process variation

Consequence:

structure variation

Effect:

electrical variation

- Variation modeling requires a hierarchical approach
 - From *ab initio* materials to devices and circuits
 - From wafer scale to feature scale
 - From process sources to electrical effects
- Model-based understanding is enabling continued variation improvement each technology generation

Experimental Data

- 1) Modeling the distribution of physical structure variation
- 2) Modeling the electrical response to a physical variation

Acknowledgements

- Kelin Kuhn, Chetan Prasad, Steve Ramey, Karson Knutson, Avner Kornfeld, Eric Karl, Zheng Guo, Mark Armstrong, Vivek Singh, Alan Myers, Gary Allen, Steve Cea, Hal Kennel, Kerrynn Foley, Tibor Grasser, Sean Ma, Justin Weber
- The many PTD, Q&R, and DTS members who contributed to the process technologies described here

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- C. Prasad, M. Agostinelli, C. Auth, S. Bodapati, M. Giles, S. Gupta, J. Hicks, K. Kuhn, K. Mistry, S. Mudanai, S. Natarajan, P. Packan, I. Post, S. Ramey, *Bias Temperature Instability Variation on SiON/Poly, HK/MG and Trigate Architectures*, submitted to IRPS 2014
- T. Grasser et al, *The Paradigm Shift in Understanding the Bias Temperature Instability: From Reaction-Diffusion to Switching Oxide Traps*, IEEE Trans. Elec. Dev. **58**(11), p. 3652, 2011.
- T. Grasser et al, *Advanced Characterization of Oxide Traps: The Dynamic Time-Dependent Defect Spectroscopy*, IRPS 2013.