

**IEEE Council on Electronic Design Automation**  
**Distinguished Lecturer Program Summary Report**

Please return completed summary report to the CEDA DLP Coordinator, Tsung-Yi Ho  
(tyho@cs.nthu.edu.tw).

<b>Organizer</b> Name: _ Marvin Chang _ Affiliation: _ National Tsing Hua University_ Email address: mfchang@ee.nthu.edu.tw	<b>Sponsoring Chapter</b> Chapter Name: _ IEEE CEDA, Taipei_ Chapter Chair: _ Iris Hui-Ru Jiang_ Email address: _ huiru.jiang@gmail.com _
<b>Event</b> Lecturer name: _ Prof. Edith Beigne (CEA-LETI) _____ Lecture topic: _ The Future of Low Power Circuits and Embedded Intelligence : Emerging Devices and New Design Paradigms _____ Location of event: _ Room 216, Delta Building, National Tsing Hua University __ Date of event: _ 13 Aug. 2018 _____ Approximate attendance: _ 40 persons (professors, students) __ If co-organized by other IEEE OU, specify here ( <i>OU and name / contact information of Chair</i> ): _ Nil. _____	

**Feedback**

Did the chapter find these slides useful? Yes
Was the technical content of the lecture(s) valuable? Yes
Was the length of the overall lecture(s) adequate? Yes
Did the audience seem responsive to the overall lecture(s)? Yes
After the lecture(s), was the lecturer available to answer any questions/comments? Yes

**Please provide any additional comments regarding this DL event.**

In the morning of Aug. 13, 2018, Prof. Beigne delivered a lecture under the support of IEEE CEDA distinguished lecturer program. After the lecture, attending professors have a joint lunch meeting with Prof. Beigne.  There were around 40 students and professors attending the lecture. After a brief overview of adaptive circuits for low power multi-processors and IoT
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architectures, she detailed new technologies opportunities for more flexibility/adaptivity; digital and mixed-signal architectures using 3D technologies were presented in the scope of multi-processors activity as well as imagers and neuro-inspired circuits. She also mentioned many AI-related researches. Her talk stimulated a lot of discussions and questions.

IEEE CEDA Taipei Chapter would like to express our gratitude to IEEE CEDA DL program and Prof. Beigne for this wonderful event including the lecture and sharing meeting.

### Photo(s) of this event

**The Future of Low Power Circuits and Embedded Intelligence : Emerging Devices and New Design Paradigms**

**講員 :** Prof. Edith Beigne(CEA-LETI)

**時間 :** 2018年8月13日 (Mon) 10:30-12:00

**地點 :** 國立清華大學 台達館216室 (Delta R216)



**Abstract** Technology variability and global environment variations are bringing many constraints on circuits and architectures today making difficult to reach high energy efficiency. After a brief overview of adaptive circuits for low power multi-processors and IoT architectures, the talk will detail new technologies opportunities for more flexibility/adaptivity. Digital and mixed-signal architectures using 3D technologies will be presented in the scope of multi-processors activity as well as imagers and neuro-inspired circuits. Also, the integration of non-volatile memories will be shown in the perspective of new architectures for computing. Finally, embedding learning will be addressed to solve power challenges at the edge and in end-devices: some new design approaches will be discussed.

**Biography** Edith Beigné joined CEA-LETI MINATEC in 1998 first working on RFID systems for biomedical applications. She focused then on asynchronous systems and circuits specifically for ultra-low power mixed-signal systems and cryptographic circuits. Since 2005, she is in charge of the low power design team within the digital laboratory developing fine-grain power control and local voltage and frequency scaling innovative features. Since 2009, her main focus is to manage power and variability issues in advanced technology nodes for high energy efficiency. She was leading complex innovative SoC design in 65nm, 32nm bulk and now in 28nm and 14nm FDSOI technologies for adaptive voltage and frequency scaling architecture based on GALS structures. Her main focus today is automatic performance regulations for ultra-low power circuits. She is part of ISSCC, ICCAD, ISLPED, DATE and ASYNC committees and JSSC editor.

