Call for Papers: Special Issue on Design and Test Solutions for Embedded Systems with Non-volatile Memories

With the rapid advances in sensing and communication technologies, embedded systems have evolved tremendously in recent years. However, embedded systems usually have limited energy, computing power, and memory/storage space. The emerging byte-addressable non-volatile memories (referred to as NVMs for short), such as Phase Change Memory (PCM), Spin-Transfer Torque RAM (STT-RAM, usually stands for STT-MRAM), Ferroelectric RAM (FRAM), and Resistive RAM (ReRAM), feature low leakage power, high density, and low unit costs. NVMs are hence popular alternatives to replace DRAM as main memory or replace hard disks and NAND flash as storage. Recently, they are even considered in the emerging processing-in-memory and computational storage designs for embedded systems.

However, NVMs fall short in some aspects such as read/write speed asymmetry and limited write cycles caused by aging and wearing issues. To tackle the issues brought by NVMs, new methodologies to design, model, and test NVMs are becoming an urgent need. In addition, the great potential of using NVM as the media of main memory and storage to build up an extra low-power embedded system has been foreseen in the near future. Thus, another urgent need is to rethink the system design and optimization issues and to rethink how to manage main memory and storage space from the viewpoint of NVMs for bringing new features in the memory hierarchy of embedded systems.

Technical papers and design perspectives from industry and academics are both welcome to be submitted to the special issue. This special issue will cover recent design techniques for various emerging NVMs, embedded systems with the support of NVMs, and their future prospects.

Topics of Interest:

Specific topics of interest include but are not limited to the following:

- Modeling and specifications for recent and emerging NVMs
- Non-volatile memory architectural designs for embedded systems
- System-level integration and optimization techniques for embedded systems with NVMs
- Prototyping and evaluation tool development for embedded systems with NVMs
- Industrial perspectives and use cases of NVMs for embedded systems

Submission Guidelines:

Prospective authors should follow the submission guidelines for IEEE Design & Test. All manuscripts must be submitted electronically to the IEEE Manuscript Central Web site at https://mc.manuscriptcentral.com/dandt, a specific special issue category will be available and selectable from a menu. All papers will undergo the standard IEEE Design & Test review process. Submitted manuscripts must not have been previously published or currently submitted for publication elsewhere.

Manuscripts must not exceed 5,000 words, including figures (with each average-size figure counting as 200 words) and a maximum of 12 references (50 for surveys). This amounts to about 4,000 words of text and a maximum of five small to medium figures. Accepted articles will be edited for clarity, structure, conciseness, grammar, passive to active voice, logical organization, readability, and adherence to style. Please see IEEE Design & Test Author Resources at http://ieee-ceda.org/publication/ieee-design-test-dt/paper-submission-instructions for links to Submission Guidelines Basics and Electronic Submission Guidelines and requirements.

Schedule:

- Manuscript submission: October 1, 2019
- First round of reviews: December 1, 2019
- Revised manuscript: January 15, 2020
- Final notification: February 15, 2020
- Final manuscript: March 15, 2020

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