



Call For Papers
Special Issue on Design and Test of Multi-Chip Packages

Aim and Scope

From auspicious beginnings over 10 years ago, the promise of 3D-IC has begun to turn the corner to more popular usage. This Special Issue on multi-chip packages focuses exclusively on design and design-for-test for three-dimensional, chiplet-based, and stacked ICs, based on through-silicon vias (TSVs), micro-bumps, and/or interposers. While these stacked ICs offer many attractive advantages with respect to heterogeneous integration, small form-factor, high bandwidth and performance, and low power dissipation, there are many open issues with respect to designing and testing such products. This issue provides a platform to present and discuss these challenges and solutions among researchers and practitioners alike.

Topics of Interest:

This special issue seeks original manuscripts that will cover innovative research and practical applications for the testability and design challenges in the following fields:

- Pure 3DIC implementations
- Other multi-chip packaging implementations including chiplets, active and passive interposers

The specific topics of interest include but are not limited to:

- Defect Detection Techniques
- DfT Architectures for 3D-ICs
- EDA Design-for-Test Flows
- Failure Analysis for 3D-ICs
- Fault-Tolerant Design for 3D-ICs
- Interposer Testing
- Known-Good Die/Stack Testing
- Standard Interfaces between Chiplets
- Methods for Power/Heat Dissipation during Test

- Pre-, Mid-, and Post-Bond Testing of 3D-ICs
- Reliability of 3D-ICs
- Improving Yield of 3D-ICs
- Redundancy & Repair
- Standards for 3D Testing, incl. IEEE Std 1838
- System/Board Test Issues for 3D-ICs
- Tester Architecture incl. ATE and BIST

The special issue particularly welcomes and encourages the submissions from industry or collaborative works between industry and academia for this fast-growing area. ***Please send your questions about the scope to the guest editors.***

Submission Guidelines:

Prospective authors should follow the submission guidelines for IEEE Design & Test. All manuscripts must be submitted electronically to IEEE Manuscript Central at <https://mc.manuscriptcentral.com/dandt>. Indicate that you are submitting your article to the special issue on Design and Test of Multi-Chip Packages. Manuscripts must not exceed 5,000 words, including figures (with each average-size figure counting as 200 words) and a maximum of 12 references (50 for surveys). This amounts to about 4,000 words of text and a maximum of five small to medium figures. Accepted articles will be edited for clarity, structure, conciseness, grammar, passive to active voice, logical organization, readability, and adherence to style. Please see IEEE Design & Test Author Information at: <https://ieee-ceda.org/publication/ieee-design-test-dt/author-info>.

Schedule:

- Submission Deadline: September 15th, 2021
- Notification First Round: December 15th, 2021
- Revision Submission: January 31st, 2022
- Final Notification: February 28th, 2022
- Final Version Due: April 1st, 2022

Guest Editors:

Please direct any questions regarding this special issue to one of the following:

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