CALL FOR PAPERS:

IEEE Journal on Exploratory Solid-State Computational Devices and Circuits special topic on "Exploratory Devices and Circuits for Compute-in-Memory"

Aims and Scope

Deep learning and non-convex optimization problems are well known to be data-intensive applications. While graphic processing units (GPU) have become the mainstream platform to accelerate the algorithms in the cloud, there is a growing interest to develop application-specific integrated-circuit (ASIC) chips for further improving the energy-efficiency for these data-intensive workloads. Digital multiply-and-accumulate (MAC) arrays are generally employed as ASIC solutions, and data flow is often optimized to increase the data reuse on-chip. Nevertheless, most of the inputs and outputs are moved across MAC arrays and from global buffers. Therefore, it is more attractive to embed the MAC computations into the memory array itself, namely *compute-in-memory (CiM)*, to minimize the data transfer. In CiM, the vector-matrix multiplication is executed in parallel (with analog computation) where the input vectors activate multiple rows. The dot-product is obtained as the multiplication of input voltage and cell conductance, and the partial sum is added up by the column current. An analog-to-digital converter (ADC) at the edge of the array generally converts the partial sum to binary bits for further digital processing.

To implement CiM, mature SRAM technologies (possibly with modified bit cells) have been proposed. However, SRAM is inherently volatile, and consumes significant standby leakage power. In this sense, emerging non-volatile memory (eNVM) technologies are better suited for the area/power constraint platforms, as they could be turned on and off instantly without losing the stored weights. eNVMs of industry's interest here include resistive random access memory (RRAM), phase change memory (PCM), spin-transfer-torque magnetic random access memory (STT-MRAM) and ferroelectric field effect transistor (FeFET). In recent years, the industry has heavily invested in the commercialization of eNVM technologies, e.g. TSMC's 40nm RRAM, Intel's 22nm RRAM, TSMC's 40nm PCM, Intel's 22nm STT-MRAM, and Samsung's 28 nm STT-MRAM, while doped HfO_2 based FeFET technology is also emerging, e.g. Globalfoundries' FeFET at 22nm.

Capitalizing on these developments, eNVM based CiM designs have also become viable. This special issue of the IEEE Journal on Exploratory Computational Devices and Circuits (JXCDC) aims to call for the recent research advances in the area of the compute-in-memory spanning devices, circuits, and systems. Papers on the interaction and co-optimization of the materials and devices as well as circuits and architecture are solicited.

Topics of Interest include but are not limited to:

Prospective authors are invited to submit original works and/or extended works based on conference presentations on various aspects of compute-in-memory. Memory technologies of interest include (but not limited to) SRAM, DRAM, NOR/NAND Flash, and emerging NVM devices such as PCM, RRAM/CBRAM, STT-MRAM/SOT-MRAM (or other spintronic memories), FeFET (or other ferroelectric memories), etc.

The following topics are specifically solicited:

- Materials and devices that can enable compute-in-memory
- Integration of emerging technologies with silicon for compute-in-memory
- Crossbar array design for compute-in-memory
- Array-level demonstration for compute-in-memory
- Peripheral circuit design for compute-in-memory
- Architectural-level design for compute-in-memory
- Algorithms and hardware co-design for compute-in-memory
- Benchmarking simulators for compute-in-memory
- New applications for compute-in-memory beyond deep learning

Submission Guidelines
The IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (JXCDC) IS AN OPEN ACCESS PUBLICATION: The Open Access Fee is: $1,350 USD per article. Article submissions must be done through the ScholarOne Manuscripts website: https://mc.manuscriptcentral.com/jxcdc.

View our guidelines for papers and supplementary materials, as well as paper templates.

Important Dates

Open for Submission: December 1st, 2019
Submission Deadline: February 1st, 2020
First Notification: March 1st, 2020
Revision Submission: April 1st, 2020
Final Decision: May 1st, 2020
Publication Online: June 1st, 2020

Guest Editor
Shimeng Yu, Georgia Institute of Technology, shimeng.yu@ece.gatech.edu

Deputy Editor
Azad Naeemi, Georgia Institute of Technology, azad@gatech.edu

Inquiries for the JxCDC Journal should be sent to: JXCDC@IEEE.ORG

JxCDC is sponsored by:

Solid-State Circuits Society
Magnetics Society
Circuits & Systems Society
Council on Electronic Design Automation
Electron Devices Society
Council on Superconductivity