IEEE Design&Test

Aim and Scope

In recent years, there has been an expedited trend in embracing bold and radical innovation of computer architectures, aiming at the continuation of computing performance improvement despite the slowed-down physical device scaling. One new frontier in the field of computing architecture is about **AI (Artificial Intelligence) hardware,** including AI hardware accelerators and neuromorphic computing processors. AI hardware has undergone a transformation from general-purpose computing to domain-specific computing (especially for deep learning applications), from Von Neumann architecture to non-Von Neumann architecture, etc. While the main focus nowadays is still functional implementation, the **testability and dependability** of these new architectures need to be addressed before the mainstream adoption of any emerging technology. The requirement for testability and dependability stems from the fact that these emerging technologies often relate to latency or throughput-critical, safety-critical, mission-critical or remotely controlled applications, i.e. computer vision, autonomous driving, smart healthcare, IoTs, robotics, etc. Testability and dependability challenges of emerging AI hardware architectures arise from many aspects, i.e. nature of computation flow and new performance goals and test metrics, in-memory and near-memory computing, high parallelism and over-provisioning, lack of fault models, lack of fault injection and fault simulation acceleration frameworks, very-large scale integration with limited test access, low observed yield of fundamental components such as memristive devices, complex propagation of faults across layers, capacity to learn around hardware-level faults, resource-constraint environment in edge devices, etc.

Topics of Interest:

This special issue seeks original manuscripts that will cover innovative research proposing solutions for the testability and dependability challenges in the following fields:

- AI hardware accelerators

- Neuromorphic computing

The specific topics of interest include but not limited to:

- Volume manufacturing test
- System-level test
- Fault modeling and fault simulation
- Pre- and post-silicon verification and debugging
- Reliability
- In-field monitoring and self-testing
- Functional safety
- Design for robustness
- Fault tolerance
- Diagnosis and failure analysis
- Yield improvement
- Failure predictive analytics
- EDA tooling
- Benchmarking

The special issue particularly welcomes and encourages the submissions from industry or collaborative works between industry and academia for this fast-growing area.

Please send your questions about the scope to the guest editors.

Submission Guidelines:

Prospective authors should follow the submission guidelines for IEEE Design & Test. All manuscripts must be submitted electronically to IEEE Manuscript Central at https://mc.manuscriptcentral.com/dandt. Indicate that you are submitting your article to the special issue on Testability and Dependability of AI Hardware. Manuscripts must not exceed 5,000 words, including figures (with each average-size figure counting as 200 words) and a maximum of 12 references (50 for surveys). This amounts to about 4,000 words of text and a maximum of five small to medium figures. Accepted articles will be edited for clarity, structure, conciseness, grammar, passive to active voice, logical organization, readability, and adherence to style. Please see IEEE Design & Test Author Information at: https://ieee-ceda.org/publication/ieee-design-test-dt/author-info.

Schedule:

- Submission Deadline: April 15th, 2021
- Notification First Round: June 15th, 2021
- Revision Submission: July 15th, 2021

- Final Notification: August 15th, 2021
- Final Version Due: September 1st, 2021

Guest Editors:

Please direct any questions regarding this special issue to one of the following:

- Fei Su, Intel Corporation, USA, fei.su@intel.com
- Chunsheng Liu, Alibaba Inc., USA, chunsheng.liu@alibaba-inc.com
- Haralampos-G. Stratigopoulos, Sorbonne Université, CNRS, LIP6, France, haralampos.stratigopoulos@lip6.fr