Call for Submissions: 2019 SVDTC Research Awards

In the field of System Validation and Debug *(organized by IEEE-CEDA SVDTC)*

SVDTC Overview

IEEE System Validation and Debug Technology Committee (SVDTC) is a body of professionals from industry and academia encompassing different organizations across the globe. This IEEE committee grew out of the observation that system validation and debug still lacks an organized effort to address the industry challenges. To this end, the SVDTC's primary focus is on fostering innovation in the field of *system validation* tools/techniques, and post-implementation debug (on silicon prototypes or emulation), where the system encompasses hardware, firmware and/or system software. The aim is to tackle broad issues that are deemed beneficial to multiple partner organizations, institutions and thus have an industry-level impact on standards, specifications, problem definitions, and so on. SVDTC is also interested to help develop a *system validation* curriculum to establish this field as an academic discipline and therefore adequately prepare the next generation of electrical and computer engineers. Further information about SVDTC can be found at https://sites.google.com/a/ieee-ceda.com/svdtc/.

Objective and Topics of Interest

The objective of this SVDTC Research Award is to recognize research undertaken by students and professionals working on system validation and debug. By promoting their research, submitters have the opportunity to raise the awareness of their work to the professional community and to enable more and stronger interactions between industry and academia. The topics of interest include but are not limited to:

- Automated post-silicon debug and validation
- Bug localization and root-cause analysis
- Compliance and compatibility validation
- Coverage metrics for post-silicon validation
- Design-for-debug and design-for-validation
- Economics of validation and debug
- Electrical validation and characterization
- On-line, in-situ, runtime validation & telemetry
- Power and performance validation
- Product validation lifecycle and planning
- Regulatory and safety validation
- Remote and secure debug (across system states)
- Requirement analysis, test content, traceability
- Thermal and reliability validation
- Validation data analytics
- Validation standardization (tools, content, etc.)

Submission Guidelines

The submission material should be included in a three-page PDF document as follows:

- One cover page
  - Researcher's name, affiliation and contact details.
  - Research project title and scope.
  - A list of publications and awards related to the research project
- Two page project description
  - Problem definition with a clear focus on system validation and debug.
  - Existing industrial practices and their limitations to address the problem.
  - Concise descriptions of the new methods, algorithms, tools, techniques, etc. developed as part of the research project and how they advance the theory and/or practice.
  - Highlights of the key results from the project and their current/anticipated impact.

The submission webpage is https://easychair.org/conferences/?conf=svdtc2019. The deadline for receiving the submissions is **December 6, 2019**. The recipient of the award will be determined by a panel of industry experts in the field of system validation and debug. The recipient will be notified on or before December 27, 2019. The award consists of two US $1,000 prizes and a certificate; one for student research, and one for professional research.